VCU108 Evaluation Board

User Guide

UG1066 (v1.5) February 6, 2019

XILINX

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/06/2019	1.5	Revised Electrostatic Discharge Caution. Added memory component information in DDR4 Component Memory. Added memory component information in RLD3 Component Memory. Revised appendix title and removed constraints file listing in Appendix D, Xilinx Design Constraints. Updated Markings in Appendix G, Regulatory and Compliance Information.
05/09/2018	1.4	Revised Figure 1-20 and Table 1-30.
11/28/2017	1.3	Updated CFP2 Module Connector. Added Documentation Navigator and Design Hubs.
07/01/2016	1.2.2	Typographical edit.
05/21/2016	1.2.1	Revised Samtec part number for FMC HPC1 Connector J2 in Table 1-1.
03/29/2016	1.2	Updated VCU108 Zynq-7000 SoC XC7Z010 System Controller in Chapter 1. Added board thickness to Dimensions in Appendix F.
10/01/2015	1.1	Updated Figure 1-2 and Figure 1-29. Updated Table 1-1 and Table 1-36. Added a second important note following Figure 1-11. Revised answer record information in Appendix G, Regulatory and Compliance Information and Appendix H, Additional Resources and Legal Notices.
07/28/2015	1.0	Initial Xilinx release.

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Appendix E: Board Setup

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Appendix G: Regulatory and Compliance Information

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VCU108 Evaluation Board Features

Overview

The VCU108 evaluation board for the Xilinx Virtex® UltraScale™ FPGA provides a hardware environment for developing and evaluating designs targeting the UltraScale XCVU095-2FFVA2104E device. The VCU108 evaluation board provides features common to many evaluation systems, including DDR4 and RLD3 component memory, a high definition multimedia interface (HDMI™), a quad small form-factor pluggable (QSFP+) connector, an eight-lane PCI Express® interface, an Ethernet PHY, general purpose I/O, and two UART interfaces. Other features can be supported using VITA-57 FPGA mezzanine cards (FMC) attached to two high pin count (HPC) FMC connectors.

Additional Resources

See Appendix H, Additional Resources and Legal Notices for references to documents, files, and resources relevant to the VCU108 board.

VCU108 Evaluation Board Features

The VCU108 evaluation board features are listed here. Detailed information for each feature is provided in VCU108 Evaluation Board Features.

- Virtex UltraScale XCVU095-2FFVA2104E FPGA
- Zynq® XC7Z010 based system controller
- Two 2.5 GB DDR4 component memory interfaces (five [256 Mb x 16] devices each)
- 144 MB RLD3 component memory interface (two [16 Mb x 36] devices)
- 1 Gb (128 MB) linear x16 BPI flash memory
- Micro secure digital (SD) connector
- USB JTAG interface using a Digilent module with micro-B USB connector

- Clock sources:
  - SI5335A quad clock generator
  - Si570 I2C programmable LVDS clock generator
  - SI5328B clock multiplier and jitter attenuator
  - Subminiature version A (SMA) connectors (differential)
- 18 GTY transceivers
  - Bull's eye SMA connector (four GTY transceivers)
  - 28 Gb/s QSFP+ connector (four GTY transceivers)
  - CFP2 connector (ten GTY transceiver)
- 28 GTH transceivers
  - 8-lane PCI Express (eight GTH transceivers)
  - FMC HPC0 connector (ten GTH transceivers)
  - FMC HPC1 connector (ten GTH transceivers)
- PCI Express endpoint connectivity
  - Gen1 8-lane (x8)
  - Gen2 8-lane (x8)
  - Gen3 8-lane (x8)
- 28 Gb/s QSFP+ connector
- CFP2 connector
- Ethernet PHY SGMII interface with RJ-45 connector
- Dual USB-to-UART bridge with micro-B USB connector
- HDMI codec with HDMI connector
- I2C bus
- Status LEDs
- User I/O
- Pmod headers
- Two VITA 57.1 FMC HPC1 connectors J2, J22
- Power management with PMBus voltage monitoring through Maxim power controllers and GUI, current monitoring using the FPGA SYSMON block.
- 10-bit 0.2 MSPS SYSMON analog-to-digital front end

- Configuration options:
  - BPI linear flash memory
  - Digilent USB configuration module
  - Platform cable USB II interface connector
  - System controller SD card to JTAG configuration

Block Diagram

The VCU108 evaluation board block diagram is shown in Figure 1-1.

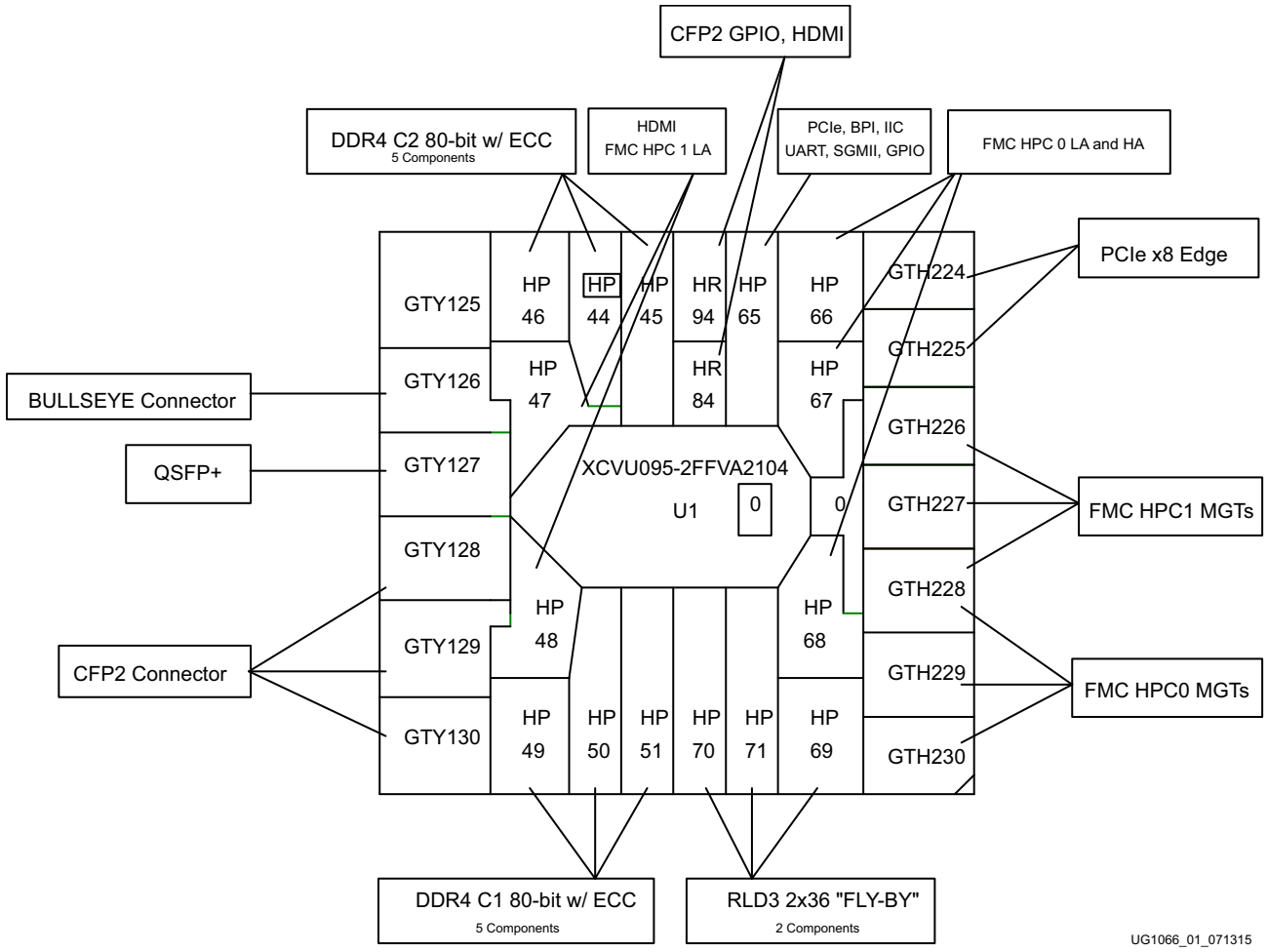


Figure 1-1: **VCU108 Evaluation Board Block Diagram**

Feature Descriptions

Figure 1-2 shows the VCU108 evaluation board. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1. Detailed information is provided starting with Virtex UltraScale XCVU095-2FFVA2104E FPGA.

IMPORTANT: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

Electrostatic Discharge Caution

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.

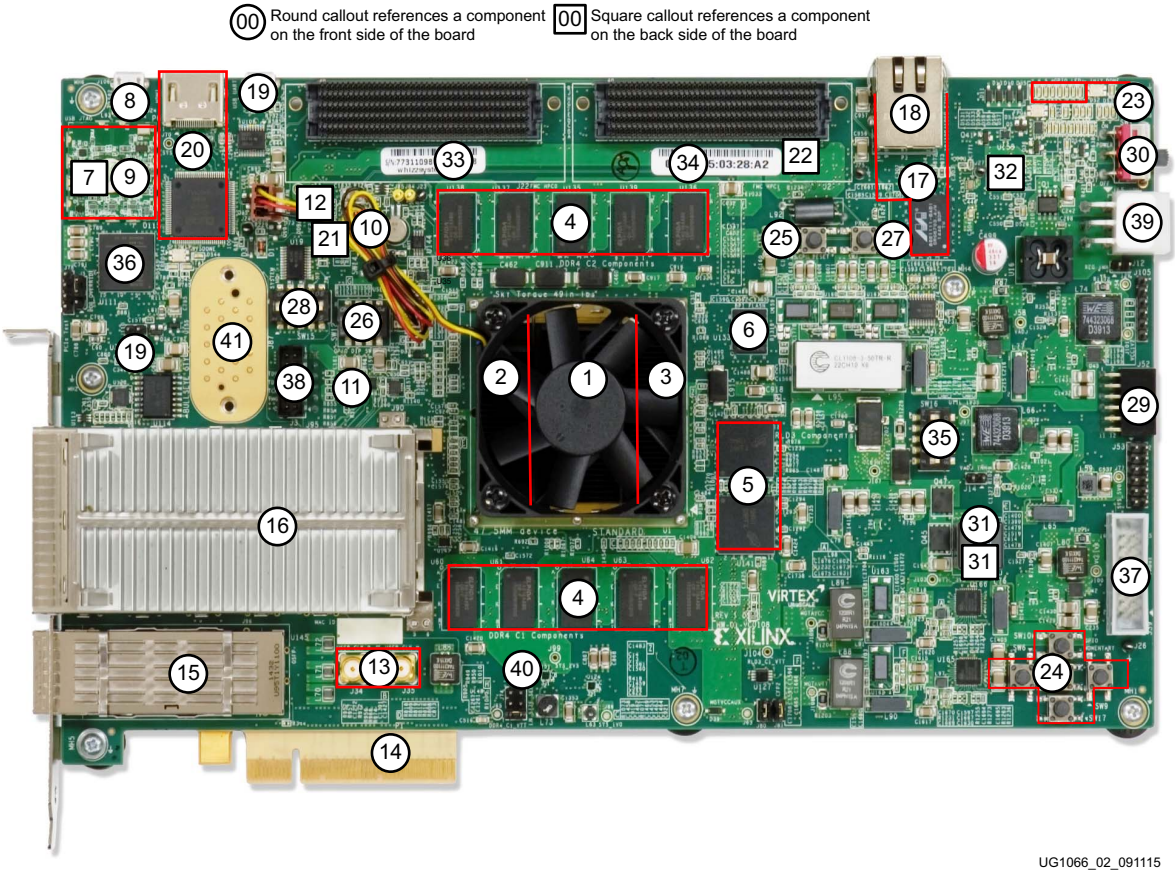


Figure 1-2: **VCU108 Board Component Locations**

Table 1-1: **VCU108 Board Component Descriptions**

Callout	Feature	Notes	Schematic 0381631 Page Number
1	Virtex UltraScale XCVU095-2FFVA2104E FPGA, (with fan-sink on soldered FPGA)	XCVU095-2FFVA2104E Cofan 30-2384-10	
2	GTY Transceivers, 6 quads	Embedded within FPGA U1	14-15
3	GTH Transceivers, 7 quads	Embedded within FPGA U1	16-17
4	DDR4 Component Memory, dual 80-bit DDR4 component memory I/F, C1 (U60-U64), C2 (U135-U139)	C1: 5 x Micron EDY4016AABG-DR-F-D, C2: 5 x Micron EDY4016AABG-DR-F-D	25-34
5	RLD3 Component Memory, RLD3 72-bit component memory I/F C3 (U141-U142)	Micron MT44K16M36RB-093E	35-36
6	Linear BPI Flash Memory, BPI 16-bit configuration memory 1Gb	Micron MT28GU01GAAA1EGC-0SIT	59
7	Micro-SD Card Interface, (bottom of board) Micro-SD card interface connector (J83)	Molex 5025700893	60

Table 1-1: **VCU108 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic 0381631 Page Number
8	USB JTAG Micro-B Connector (J106) (see Digilent USB JTAG Module)	Hirose ZX62D-AB-5P8	24
9	Digilent USB JTAG Module (U115), with Micro-B connector	Digilent JTAG-SMT2-NC	24
10	System Clock, multi-output clock generator, SYSCLK and other clocks, 1.8V LVDS (U122)	SI5335A-B02436-GM, 4 outputs: 300 MHz, 125 MHz, 90 MHz, 33.33 MHz	47
11	Programmable User Clock, programmable user clock, I2C programmable user clock, 3.3V LVDS (U32) with 1-to-2 LVDS buffer (U104)	Silicon Labs SI570BAB0000544DG (default 156.250 MHz) with Si53340 buffer	48
12	Jitter Attenuated Clock, jitter attenuated clock (U57) (bottom of board)	Silicon Labs SI5328B-C-GMR	57
13	User SMA Clock, user differential SMA clock P/N (J34/J35)	Rosenberger 32K10K-400L5	56
14	PCI Express Endpoint Connectivity, PCI Express connector (P1)	8-lane card edge connector	46
15	28 Gb/s QSFP+ Module Connector, (U145)	Amphenol FS1-Z38-20Z6-10	53
16	CFP2 Module Connector, (J89)	Yamaichi CH1215-104-0001	54
17	10/100/1000 Mb/s Tri-Speed Ethernet PHY with RJ45, SGMII mode only, (U58,P3)	Marvell M88E1111-BAB1C000 with Halo HFJ11-1G01E-L12RL RJ45	58
18	Ethernet PHY Status LEDs, LEDs are integrated into P3 bezel	Halo HFJ11-1G01E-L12RL RJ45 integrated status LEDs (Rev B)	58
19	Dual USB-to-UART Bridge, bridge device (U34) with mini-B connector (J4)	Silicon Labs CP2105-F01-GM bridge, Hirose ZX62D-AB-5P8 connector	61
20	HDMI Video Output, HDMI controller (U52), HDMI connector (P6)	Analog devices ADV7511KSTZ-P, Molex 538-47151-001	67-68
21	I2C Bus, Topology, and Switches, I2C bus, I2C bus MUX (U28) (bottom of board)	TI TCA9548APWR	70
22	I2C Bus, Topology, and Switches, I2C bus, I2C bus MUX (U80) (bottom of board)	TI PCA9544ARGYR	70
23	User GPIO LEDs (DS6-DS10, DS31-DS33) VCU108 Board Status and User LEDs, Table 1-31	GPIO LEDs, green 0603 Lumex SML-LX0603GW-TR	62
24	User Pushbuttons, active-High (SW6-SW10)	E-Switch TL3301EF100QG in north, south, east, west, center pattern	62
25	CPU Reset Pushbutton, user CPU RESET, active-High (SW5)	E-Switch TL3301EF100QG	62
26	GPIO DIP Switch, GPIO DIP switch (SW12)	4-pole C&K SDA04H1SBD	62
27	Program_B Pushbutton Switch, FPGA PROG pushbutton (SW4)	E-Switch TL3301EF100QG	62

Table 1-1: **VCU108 Board Component Descriptions *(Cont'd)***

Callout	Feature	Notes	Schematic 0381631 Page Number
28	VCU108 Zynq-7000 SoC XC7Z010 System Controller, mode switch DIP switch (SW15)	5-pole C&K SDA05H1SBD	52
29	User Pmod GPIO Headers, Pmod headers (J52,J53) with level shifters (U41,U42)	J52 2x6 0.1 female rt-angle receptacle Sullins PPPC062LJBN-RC, J53 2x6 0.1 male header Sullins PBC36DAAN; TI TXS0108EPWR	69
30	Power On/Off Slide Switch SW1	C&K 1201M2S3AQE2	72
31	VCU108 Board Power System, power management system (top and bottom)	Maxim MAX15301 and MAX15303 digital P.O.L. controllers	73-86
32	Monitoring Voltage and Current, power management voltage and current sensing SYSMON external circuitry	Analog devices MUX ADG707BRUZ TI operational amplifiers INA333AIDGKR	65-66
33	FMC HPC0 Connector J22	Samtec ASP_134486_01	38-41
34	FMC HPC1 Connector J2	Samtec ASP_134486_01	42-45
35	FPGA U1 Configuration MODE DIP switch (see Configuration Options), (SW16)	5-pole C&K SDA05H1SBD	3
36	VCU108 Zynq-7000 SoC XC7Z010 System Controller, Zynq-7000 SoC XC7Z010CLG225 (U111)	XC7Z010CLG225	49-52
37	Monitoring Voltage and Current, 2x8 shrouded PMBus connector (J39)	ASSMAN AWHW16G-0202	71
38	Digilent USB JTAG Module, 2x7, 2 mm shrouded JTAG cable connector (J3)	Molex 87832-1420	24
39	Power On/Off Slide Switch SW1, (J15)	Molex-39-30-1060	72
40	PCI Express Endpoint Connectivity, PCIe lane width select header, (J74)	2x3 0.1 inch male header Sullins PBC36DAAN	46
41	GTY Transceivers, Samtec bull's eye connector SMT pad, (J87)	Samtec HDR-155805-01	56

Notes:

1. The VCU108 board schematics are available for download. See the VCU108 Evaluation Kit.
2. The VCU108 board jumper header locations are shown in Figure A-1.

Virtex UltraScale XCVU095-2FFVA2104E FPGA

[Figure 1-2, callout 1]

The VCU108 board is populated with the Virtex UltraScale XCVU095-2FFVA2104E FPGA.

For further information on Virtex UltraScale FPGAs, see V*irtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893) [Ref 1].

FPGA Configuration

The VCU108 board supports two of the five UltraScale FPGA configuration modes:

- Master BPI using the onboard linear BPI flash memory
- JTAG using:
  - USB JTAG configuration port (Digilent module U115)
  - Platform cable USB 2.0, 2 mm, keyed flat cable header (J3)
  - System controller from SD card

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW16 positions 3, 4, and 5, respectively, as shown in Figure 1-3. The FPGA default mode setting M[2:0] = **101** selects the JTAG configuration mode.

Table 1-2: **VCU108 Board FPGA Configuration Modes**

Configuration Mode	SW16 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master BPI	010	x8, x16	Output
JTAG	101	x1	Not applicable

For full details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2].

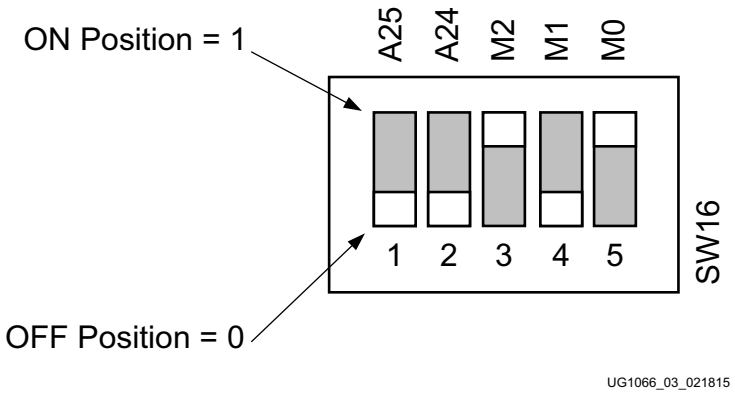


Figure 1-3: SW16 Default Settings

Encryption Key Backup Circuit

The XCVU095 FPGA U1 implements bitstream encryption key technology. The VCU108 board provides the encryption key backup battery circuit shown in Figure 1-4. The Seiko TS518FE rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the XCVU095 FPGA U1 VCCBATT pin AT11. The battery supply current IBATT specification is 150 nA max when board power is off. B1 is charged from the SYS_1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 KΩ current limit resistor. The nominal charging voltage is 1.42V. Figure 1-4 shows the encryption key battery backup circuit.

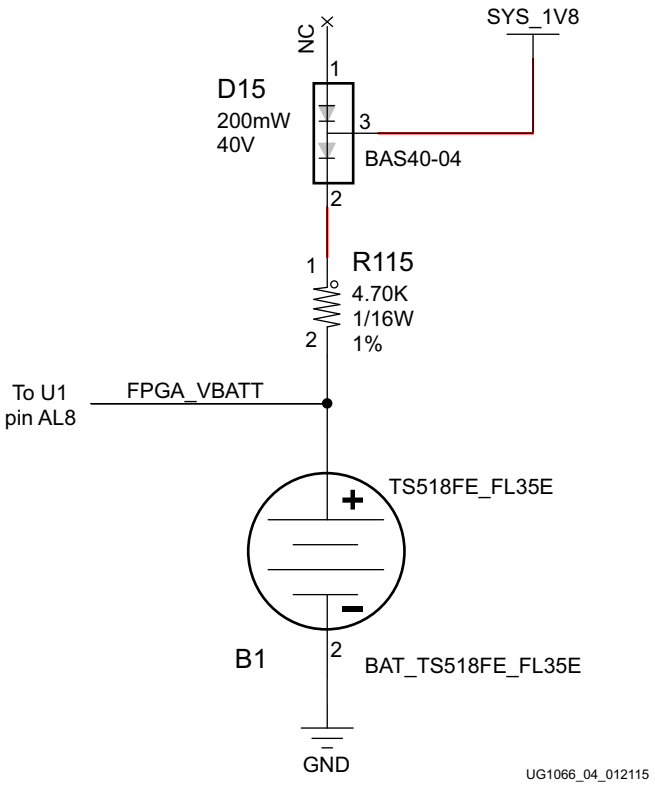


Figure 1-4: **Encryption Key Backup Circuit**

I/O Voltage Rails

There are 17 I/O banks available on the XCVCU095 device and the VCU108 board. The voltages applied to the FPGA I/O banks (shown in Figure 1-5) used by the VCU108 board are listed in Table 1-3.

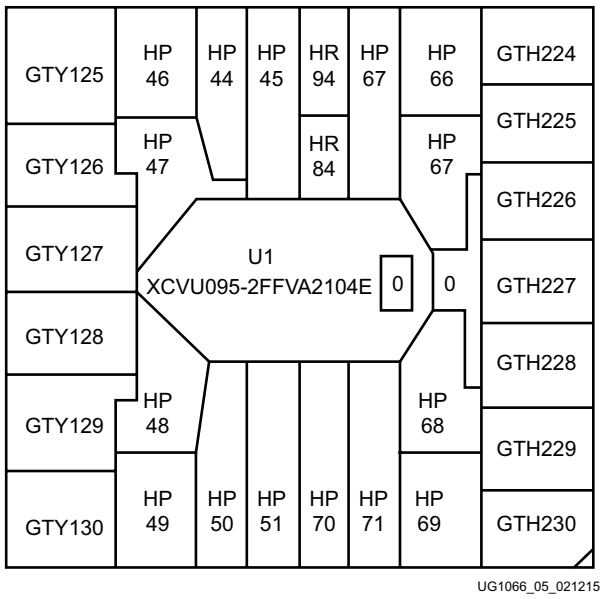


Figure 1-5: **UltraScale XCVU095 Bank Locations**

Table 1-3: **I/O Bank Voltage Rails**

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
Bank 0	VCC1V8_FPGA	1.8V
HP Bank 44	VCC1V2_FPGA	1.2V
HP Bank 45	VCC1V2_FPGA	1.2V
HP Bank 46	VCC1V2_FPGA	1.2V
HP Bank 47	VADJ_1V8_FPGA	1.8V
HP Bank 48	VADJ_1V8_FPGA	1.8V
HP Bank 49	VCC1V2_FPGA	1.2V
HP Bank 50	VCC1V2_FPGA	1.2V
HP Bank 51	VCC1V2_FPGA	1.2V
HP Bank 65	VCC1V8_FPGA	1.8V
HP Bank 66	VADJ_1V8_FPGA	1.8V
HP Bank 67	VADJ_1V8_FPGA	1.8V
HP Bank 68	VADJ_1V8_FPGA	1.8V
HP Bank 69	VCC1V2_FPGA	1.2V

Table 1-3: **I/O Bank Voltage Rails *(Cont'd)***

FPGA (U1) Bank	Power Supply Rail Net Name	Voltage
HP Bank 70	VCC1V2_FPGA	1.2V
HP Bank 71	VCC1V2_FPGA	1.2V
HR Bank 84	VCC1V8_FPGA	1.8V
HR Bank 94	VCC1V8_FPGA	1.8V

DDR4 Component Memory

[Figure 1-2, callout 4]

The dual 4 GB DDR4 component memory system is comprised of two sets of five 256 Mb x 16 DDR4 SDRAM devices located at U60-U64 (C1) and U135-U139 (C2).

- Manufacturer: Micron
- Part number: EDY4016AABG-DR-F-D
- Configuration: 2Gb: 256 Mb x 16
- Supply voltage: 1.5V
- Datapath width: 32 bits
- Data rate: Up to 1,333 MT/s

The VCU108 XCVU095 FPGA DDR interface performance is documented in the *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (UG893) [Ref 1].

This memory system is connected to the XCVU095 HP banks 49, 50, and 51 (C1), and 44, 45, and 46 (C2). The DDR4 0.6V VTT termination voltages (nets DDR4_C1_VTTand DDR4_C2_VTT) are sourced from TI TPS51200DR linear regulators U24 and U134. The DDR4 memory interface banks U60-U64 (C1) and U135-139 (C2) VREF pins are wired to GND through 1K resistors, invoking the INTERNAL VREF mode. The connections between the C1 interface DDR4 component memories and XCVU095 banks 49, 50, and 51 are listed in Table 1-4.

Table 1-4: **DDR4 Memory 80-bit I/F C1 to FPGA U1 Banks 49, 50, and 51**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
J37	DDR4_C1_DQ0	POD12_DCI	G2	DQL0	U60
H40	DDR4_C1_DQ1	POD12_DCI	F7	DQL1	U60
F38	DDR4_C1_DQ2	POD12_DCI	H3	DQL2	U60
H39	DDR4_C1_DQ3	POD12_DCI	H7	DQL3	U60
K37	DDR4_C1_DQ4	POD12_DCI	H2	DQL4	U60

Table 1-4: **DDR4 Memory 80-bit I/F C1 to FPGA U1 Banks 49, 50, and 51 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
G40	DDR4_C1_DQ5	POD12_DCI	H8	DQL5	U60
F39	DDR4_C1_DQ6	POD12_DCI	J3	DQL6	U60
F40	DDR4_C1_DQ7	POD12_DCI	J7	DQL7	U60
F36	DDR4_C1_DQ8	POD12_DCI	A3	DQU0	U60
J36	DDR4_C1_DQ9	POD12_DCI	B8	DQU1	U60
F35	DDR4_C1_DQ10	POD12_DCI	C3	DQU2	U60
J35	DDR4_C1_DQ11	POD12_DCI	C7	DQU3	U60
G37	DDR4_C1_DQ12	POD12_DCI	C2	DQU4	U60
H35	DDR4_C1_DQ13	POD12_DCI	C8	DQU5	U60
G36	DDR4_C1_DQ14	POD12_DCI	D3	DQU6	U60
H37	DDR4_C1_DQ15	POD12_DCI	D7	DQU7	U60
H38	DDR4_C1_DQS0_T	DIFF_POD12_DCI	G3	DQSL_T	U60
G38	DDR4_C1_DQS0_C	DIFF_POD12_DCI	F3	DQSL_C	U60
H34	DDR4_C1_DQS1_T	DIFF_POD12_DCI	B7	DQSU_T	U60
G35	DDR4_C1_DQS1_C	DIFF_POD12_DCI	A7	DQSU_C	U60
J39	DDR4_C1_DM0	POD12_DCI	E7	DML_B/DBIL_B	U60
F34	DDR4_C1_DM1	POD12_DCI	E2	DMU_B/DBIU_B	U60
C39	DDR4_C1_DQ16	POD12_DCI	G2	DQL0	U61
A38	DDR4_C1_DQ17	POD12_DCI	F7	DQL1	U61
B40	DDR4_C1_DQ18	POD12_DCI	H3	DQL2	U61
D40	DDR4_C1_DQ19	POD12_DCI	H7	DQL3	U61
E38	DDR4_C1_DQ20	POD12_DCI	H2	DQL4	U61
B38	DDR4_C1_DQ21	POD12_DCI	H8	DQL5	U61
E37	DDR4_C1_DQ22	POD12_DCI	J3	DQL6	U61
C40	DDR4_C1_DQ23	POD12_DCI	J7	DQL7	U61
C34	DDR4_C1_DQ24	POD12_DCI	A3	DQU0	U61
A34	DDR4_C1_DQ25	POD12_DCI	B8	DQU1	U61
D34	DDR4_C1_DQ26	POD12_DCI	C3	DQU2	U61
A35	DDR4_C1_DQ27	POD12_DCI	C7	DQU3	U61
A36	DDR4_C1_DQ28	POD12_DCI	C2	DQU4	U61
C35	DDR4_C1_DQ29	POD12_DCI	C8	DQU5	U61
B35	DDR4_C1_DQ30	POD12_DCI	D3	DQU6	U61
D35	DDR4_C1_DQ31	POD12_DCI	D7	DQU7	U61
A39	DDR4_C1_DQS2_T	DIFF_POD12_DCI	G3	DQSL_C	U61

Table 1-4: **DDR4 Memory 80-bit I/F C1 to FPGA U1 Banks 49, 50, and 51 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
A40	DDR4_C1_DQS2_C	DIFF_POD12_DCI	F3	DQSL_T	U61
B36	DDR4_C1_DQS3_T	DIFF_POD12_DCI	B7	DQSU_C	U61
B37	DDR4_C1_DQS3_C	DIFF_POD12_DCI	A7	DQSU_T	U61
E39	DDR4_C1_DM2	POD12_DCI	E7	DML_B/DBIL_B	U61
D37	DDR4_C1_DM3	POD12_DCI	E2	DMU_B/DBIU_B	U61
N27	DDR4_C1_DQ32	POD12_DCI	G2	DQL0	U62
R27	DDR4_C1_DQ33	POD12_DCI	F7	DQL1	U62
N24	DDR4_C1_DQ34	POD12_DCI	H3	DQL2	U62
R24	DDR4_C1_DQ35	POD12_DCI	H7	DQL3	U62
P24	DDR4_C1_DQ36	POD12_DCI	H2	DQL4	U62
P26	DDR4_C1_DQ37	POD12_DCI	H8	DQL5	U62
P27	DDR4_C1_DQ38	POD12_DCI	J3	DQL6	U62
T24	DDR4_C1_DQ39	POD12_DCI	J7	DQL7	U62
K27	DDR4_C1_DQ40	POD12_DCI	A3	DQU0	U62
L26	DDR4_C1_DQ41	POD12_DCI	B8	DQU1	U62
J27	DDR4_C1_DQ42	POD12_DCI	C3	DQU2	U62
K28	DDR4_C1_DQ43	POD12_DCI	C7	DQU3	U62
K26	DDR4_C1_DQ44	POD12_DCI	C2	DQU4	U62
M25	DDR4_C1_DQ45	POD12_DCI	C8	DQU5	U62
J26	DDR4_C1_DQ46	POD12_DCI	D3	DQU6	U62
L28	DDR4_C1_DQ47	POD12_DCI	D7	DQU7	U62
P25	DDR4_C1_DQS4_T	DIFF_POD12_DCI	G3	DQSL_C	U62
N25	DDR4_C1_DQS4_C	DIFF_POD12_DCI	F3	DQSL_T	U62
L24	DDR4_C1_DQS5_T	DIFF_POD12_DCI	B7	DQSU_C	U62
L25	DDR4_C1_DQS5_C	DIFF_POD12_DCI	A7	DQSU_T	U62
T26	DDR4_C1_DM4	POD12_DCI	E7	DML_B/DBIL_B	U62
M27	DDR4_C1_DM5	POD12_DCI	E2	DMU_B/DBIU_B	U62
E27	DDR4_C1_DQ48	POD12_DCI	G2	DQL0	U63
E28	DDR4_C1_DQ49	POD12_DCI	F7	DQL1	U63
E26	DDR4_C1_DQ50	POD12_DCI	H3	DQL2	U63
H27	DDR4_C1_DQ51	POD12_DCI	H7	DQL3	U63
F25	DDR4_C1_DQ52	POD12_DCI	H2	DQL4	U63
F28	DDR4_C1_DQ53	POD12_DCI	H8	DQL5	U63
G25	DDR4_C1_DQ54	POD12_DCI	J3	DQL6	U63

Table 1-4: **DDR4 Memory 80-bit I/F C1 to FPGA U1 Banks 49, 50, and 51 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
G27	DDR4_C1_DQ55	POD12_DCI	J7	DQL7	U63
B28	DDR4_C1_DQ56	POD12_DCI	A3	DQU0	U63
A28	DDR4_C1_DQ57	POD12_DCI	B8	DQU1	U63
B25	DDR4_C1_DQ58	POD12_DCI	C3	DQU2	U63
B27	DDR4_C1_DQ59	POD12_DCI	C7	DQU3	U63
D25	DDR4_C1_DQ60	POD12_DCI	C2	DQU4	U63
C27	DDR4_C1_DQ61	POD12_DCI	C8	DQU5	U63
C25	DDR4_C1_DQ62	POD12_DCI	D3	DQU6	U63
D26	DDR4_C1_DQ63	POD12_DCI	D7	DQU7	U63
H28	DDR4_C1_DQS6_T	DIFF_POD12_DCI	G3	DQSL_C	U63
G28	DDR4_C1_DQS6_C	DIFF_POD12_DCI	F3	DQSL_T	U63
B26	DDR4_C1_DQS7_T	DIFF_POD12_DCI	B7	DQSU_C	U63
A26	DDR4_C1_DQS7_C	DIFF_POD12_DCI	A7	DQSU_T	U63
G26	DDR4_C1_DM6	POD12_DCI	E7	DML_B/DBIL_B	U63
D27	DDR4_C1_DM7	POD12_DCI	E2	DMU_B/DBIU_B	U63
N29	DDR4_C1_DQ64	POD12_DCI	G2	DQL0	U64
M31	DDR4_C1_DQ65	POD12_DCI	F7	DQL1	U64
P29	DDR4_C1_DQ66	POD12_DCI	H3	DQL2	U64
L29	DDR4_C1_DQ67	POD12_DCI	H7	DQL3	U64
P30	DDR4_C1_DQ68	POD12_DCI	H2	DQL4	U64
N28	DDR4_C1_DQ69	POD12_DCI	H8	DQL5	U64
L31	DDR4_C1_DQ70	POD12_DCI	J3	DQL6	U64
L30	DDR4_C1_DQ71	POD12_DCI	J7	DQL7	U64
H30	DDR4_C1_DQ72	POD12_DCI	A3	DQU0	U64
J32	DDR4_C1_DQ73	POD12_DCI	B8	DQU1	U64
H29	DDR4_C1_DQ74	POD12_DCI	C3	DQU2	U64
H32	DDR4_C1_DQ75	POD12_DCI	C7	DQU3	U64
J29	DDR4_C1_DQ76	POD12_DCI	C2	DQU4	U64
K32	DDR4_C1_DQ77	POD12_DCI	C8	DQU5	U64
J30	DDR4_C1_DQ78	POD12_DCI	D3	DQU6	U64
G32	DDR4_C1_DQ79	POD12_DCI	D7	DQU7	U64
N30	DDR4_C1_DQS8_T	DIFF_POD12_DCI	G3	DQSL_C	U64
M30	DDR4_C1_DQS8_C	DIFF_POD12_DCI	F3	DQSL_T	U64
H33	DDR4_C1_DQS9_T	DIFF_POD12_DCI	B7	DQSU_C	U64

Table 1-4: **DDR4 Memory 80-bit I/F C1 to FPGA U1 Banks 49, 50, and 51 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
G33	DDR4_C1_DQS9_C	DIFF_POD12_DCI	A7	DQSU_T	U64
R28	DDR4_C1_DM8	POD12_DCI	E7	DML_B/DBIL_B	U64
K31	DDR4_C1_DM9	POD12_DCI	E2	DMU_B/DBIU_B	U64
C30	DDR4_C1_A0	SSTL12_DCI	P3	A0	U60-U64
D32	DDR4_C1_A1	SSTL12_DCI	P7	A1	U60-U64
B30	DDR4_C1_A2	SSTL12_DCI	R3	A2	U60-U64
C33	DDR4_C1_A3	SSTL12_DCI	N7	A3	U60-U64
E32	DDR4_C1_A4	SSTL12_DCI	N3	A4	U60-U64
A29	DDR4_C1_A5	SSTL12_DCI	P8	A5	U60-U64
C29	DDR4_C1_A6	SSTL12_DCI	P2	A6	U60-U64
E29	DDR4_C1_A7	SSTL12_DCI	R8	A7	U60-U64
A30	DDR4_C1_A8	SSTL12_DCI	R2	A8	U60-U64
C32	DDR4_C1_A9	SSTL12_DCI	R7	A9	U60-U64
A31	DDR4_C1_A10	SSTL12_DCI	M3	A10/AP	U60-U64
A33	DDR4_C1_A11	SSTL12_DCI	T2	A11	U60-U64
F29	DDR4_C1_A12	SSTL12_DCI	M7	A12/BC_B	U60-U64
B32	DDR4_C1_A13	SSTL12_DCI	T8	A13	U60-U64
G30	DDR4_C1_BA0	SSTL12_DCI	N2	BA0	U60-U64
F30	DDR4_C1_BA1	SSTL12_DCI	N8	BA1	U60-U64
F33	DDR4_C1_BG0	SSTL12_DCI	M2	BG0	U60-U64
D29	DDR4_C1_A14_WE_B	SSTL12_DCI	L2	WE_B/A14	U60-U64
B31	DDR4_C1_A15_CAS_B	SSTL12_DCI	M8	CAS_B_A15	U60-U64
B33	DDR4_C1_A16_RAS_B	SSTL12_DCI	L8	RAS_B/A16	U60-U64
E31	DDR4_C1_CK_T	DIFF_SSTL12_DCI	K7	CK_T	U60-U64
D31	DDR4_C1_CK_C	DIFF_SSTL12_DCI	K8	CK_C	U60-U64
K29	DDR4_C1_CKE	SSTL12_DCI	K2	CKE	U60-U64
E33	DDR4_C1_ACT_B	SSTL12_DCI	L3	ACT_B	U60-U64
R29	DDR4_C1_PAR	SSTL12_DCI	T3	PAR	U60-U64
J31	DDR4_C1_ODT	SSTL12_DCI	K3	ODT	U60-U64
D30	DDR4_C1_CS_B	SSTL12_DCI	L7	CS_B	U60-U64
J40	DDR4_C1_ALERT_B	SSTL12_DCI	P9	ALERT_B	U60-U64
M28	DDR4_C1_RESET_B	LVCMOS12	P1	RESET_B	U60-U64

The connections between the C2 interface DDR4 component memories (U135-U139) and XCVU095 banks 44, 45, and 46 are listed in Table 1-5.

Table 1-5: **DDR4 Memory 80-bit I/F C2 to FPGA U1 Banks 44, 45, and 46**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref.Des.
BE30	DDR4_C2_DQ0	POD12_DCI	G2	DQL0	U135
BE33	DDR4_C2_DQ1	POD12_DCI	F7	DQL1	U135
BD30	DDR4_C2_DQ2	POD12_DCI	H3	DQL2	U135
BD33	DDR4_C2_DQ3	POD12_DCI	H7	DQL3	U135
BD31	DDR4_C2_DQ4	POD12_DCI	H2	DQL4	U135
BC33	DDR4_C2_DQ5	POD12_DCI	H8	DQL5	U135
BD32	DDR4_C2_DQ6	POD12_DCI	J3	DQL6	U135
BC31	DDR4_C2_DQ7	POD12_DCI	J7	DQL7	U135
BA31	DDR4_C2_DQ8	POD12_DCI	A3	DQU0	U135
AY33	DDR4_C2_DQ9	POD12_DCI	B8	DQU1	U135
BA30	DDR4_C2_DQ10	POD12_DCI	C3	DQU2	U135
AW31	DDR4_C2_DQ11	POD12_DCI	C7	DQU3	U135
AW32	DDR4_C2_DQ12	POD12_DCI	C2	DQU4	U135
BB33	DDR4_C2_DQ13	POD12_DCI	C8	DQU5	U135
AY32	DDR4_C2_DQ14	POD12_DCI	D3	DQU6	U135
BA32	DDR4_C2_DQ15	POD12_DCI	D7	DQU7	U135
BF30	DDR4_C2_DQS0_T	DIFF_POD12_DCI	G3	DQSL_T	U135
BF31	DDR4_C2_DQS0_C	DIFF_POD12_DCI	F3	DQSL_C	U135
AY34	DDR4_C2_DQS1_T	DIFF_POD12_DCI	B7	DQSU_T	U135
BA34	DDR4_C2_DQS1_C	DIFF_POD12_DCI	A7	DQSU_C	U135
BE32	DDR4_C2_DM0	POD12_DCI	E7	DML_B/DBIL_B	U135
BB31	DDR4_C2_DM1	POD12_DCI	E2	DMU_B/DBIU_B	U135
AT31	DDR4_C2_DQ16	POD12_DCI	G2	DQL0	U136
AV31	DDR4_C2_DQ17	POD12_DCI	F7	DQL1	U136
AV30	DDR4_C2_DQ18	POD12_DCI	H3	DQL2	U136
AU33	DDR4_C2_DQ19	POD12_DCI	H7	DQL3	U136
AU31	DDR4_C2_DQ20	POD12_DCI	H2	DQL4	U136
AU32	DDR4_C2_DQ21	POD12_DCI	H8	DQL5	U136
AW30	DDR4_C2_DQ22	POD12_DCI	J3	DQL6	U136
AU34	DDR4_C2_DQ23	POD12_DCI	J7	DQL7	U136
AT29	DDR4_C2_DQ24	POD12_DCI	A3	DQU0	U136

Table 1-5: **DDR4 Memory 80-bit I/F C2 to FPGA U1 Banks 44, 45, and 46 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref.Des.
AT34	DDR4_C2_DQ25	POD12_DCI	B8	DQU1	U136
AT30	DDR4_C2_DQ26	POD12_DCI	C3	DQU2	U136
AR33	DDR4_C2_DQ27	POD12_DCI	C7	DQU3	U136
AR30	DDR4_C2_DQ28	POD12_DCI	C2	DQU4	U136
AN30	DDR4_C2_DQ29	POD12_DCI	C8	DQU5	U136
AP30	DDR4_C2_DQ30	POD12_DCI	D3	DQU6	U136
AN31	DDR4_C2_DQ31	POD12_DCI	D7	DQU7	U136
AU29	DDR4_C2_DQS2_T	DIFF_POD12_DCI	G3	DQSL_C	U136
AV29	DDR4_C2_DQS2_C	DIFF_POD12_DCI	F3	DQSL_T	U136
AP31	DDR4_C2_DQS3_T	DIFF_POD12_DCI	B7	DQSU_C	U136
AP32	DDR4_C2_DQS3_C	DIFF_POD12_DCI	A7	DQSU_T	U136
AV33	DDR4_C2_DM2	POD12_DCI	E7	DML_B/DBIL_B	U136
AR32	DDR4_C2_DM3	POD12_DCI	E2	DMU_B/DBIU_B	U136
BF34	DDR4_C2_DQ32	POD12_DCI	G2	DQL0	U137
BF36	DDR4_C2_DQ33	POD12_DCI	F7	DQL1	U137
BC35	DDR4_C2_DQ34	POD12_DCI	H3	DQL2	U137
BE37	DDR4_C2_DQ35	POD12_DCI	H7	DQL3	U137
BE34	DDR4_C2_DQ36	POD12_DCI	H2	DQL4	U137
BD36	DDR4_C2_DQ37	POD12_DCI	H8	DQL5	U137
BF37	DDR4_C2_DQ38	POD12_DCI	J3	DQL6	U137
BC36	DDR4_C2_DQ39	POD12_DCI	J7	DQL7	U137
BD37	DDR4_C2_DQ40	POD12_DCI	A3	DQU0	U137
BE38	DDR4_C2_DQ41	POD12_DCI	B8	DQU1	U137
BD38	DDR4_C2_DQ42	POD12_DCI	C3	DQU2	U137
BD40	DDR4_C2_DQ43	POD12_DCI	C7	DQU3	U137
BB38	DDR4_C2_DQ44	POD12_DCI	C2	DQU4	U137
BB39	DDR4_C2_DQ45	POD12_DCI	C8	DQU5	U137
BC39	DDR4_C2_DQ46	POD12_DCI	D3	DQU6	U137
BC38	DDR4_C2_DQ47	POD12_DCI	D7	DQU7	U137
BE35	DDR4_C2_DQS4_T	DIFF_POD12_DCI	G3	DQSL_T	U137
BF35	DDR4_C2_DQS4_C	DIFF_POD12_DCI	F3	DQSL_C	U137
BE39	DDR4_C2_DQS5_T	DIFF_POD12_DCI	B7	DQSU_T	U137
BF39	DDR4_C2_DQS5_C	DIFF_POD12_DCI	A7	DQSU_C	U137
BC34	DDR4_C2_DM4	POD12_DCI	E7	DML_B/DBIL_B	U137

Table 1-5: **DDR4 Memory 80-bit I/F C2 to FPGA U1 Banks 44, 45, and 46 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref.Des.
BE40	DDR4_C2_DM5	POD12_DCI	E2	DMU_B/DBIU_B	U137
AW40	DDR4_C2_DQ48	POD12_DCI	G2	DQL0	U138
BA40	DDR4_C2_DQ49	POD12_DCI	F7	DQL1	U138
AY39	DDR4_C2_DQ50	POD12_DCI	H3	DQL2	U138
AY38	DDR4_C2_DQ51	POD12_DCI	H7	DQL3	U138
AY40	DDR4_C2_DQ52	POD12_DCI	H2	DQL4	U138
BA39	DDR4_C2_DQ53	POD12_DCI	H8	DQL5	U138
BB36	DDR4_C2_DQ54	POD12_DCI	J3	DQL6	U138
BB37	DDR4_C2_DQ55	POD12_DCI	J7	DQL7	U138
AV38	DDR4_C2_DQ56	POD12_DCI	A3	DQU0	U138
AU38	DDR4_C2_DQ57	POD12_DCI	B8	DQU1	U138
AU39	DDR4_C2_DQ58	POD12_DCI	C3	DQU2	U138
AW35	DDR4_C2_DQ59	POD12_DCI	C7	DQU3	U138
AU40	DDR4_C2_DQ60	POD12_DCI	C2	DQU4	U138
AV40	DDR4_C2_DQ61	POD12_DCI	C8	DQU5	U138
AW36	DDR4_C2_DQ62	POD12_DCI	D3	DQU6	U138
AV39	DDR4_C2_DQ63	POD12_DCI	D7	DQU7	U138
BA35	DDR4_C2_DQS6_T	DIFF_POD12_DCI	G3	DQSL_C	U138
BA36	DDR4_C2_DQS6_C	DIFF_POD12_DCI	F3	DQSL_T	U138
AW37	DDR4_C2_DQS7_T	DIFF_POD12_DCI	B7	DQSU_C	U138
AW38	DDR4_C2_DQS7_C	DIFF_POD12_DCI	A7	DQSU_T	U138
AY37	DDR4_C2_DM6	POD12_DCI	E7	DML_B/DBIL_B	U138
AV35	DDR4_C2_DM7	POD12_DCI	E2	DMU_B/DBIU_B	U138
BD25	DDR4_C2_DQ64	POD12_DCI	G2	DQL0	U139
BD26	DDR4_C2_DQ65	POD12_DCI	F7	DQL1	U139
BD27	DDR4_C2_DQ66	POD12_DCI	H3	DQL2	U139
BE27	DDR4_C2_DQ67	POD12_DCI	H7	DQL3	U139
BD28	DDR4_C2_DQ68	POD12_DCI	H2	DQL4	U139
BE28	DDR4_C2_DQ69	POD12_DCI	H8	DQL5	U139
BF26	DDR4_C2_DQ70	POD12_DCI	J3	DQL6	U139
BF27	DDR4_C2_DQ71	POD12_DCI	J7	DQL7	U139
AY27	DDR4_C2_DQ72	POD12_DCI	A3	DQU0	U139
BC26	DDR4_C2_DQ73	POD12_DCI	B8	DQU1	U139
BA27	DDR4_C2_DQ74	POD12_DCI	C3	DQU2	U139

Table 1-5: **DDR4 Memory 80-bit I/F C2 to FPGA U1 Banks 44, 45, and 46 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref.Des.
BB28	DDR4_C2_DQ75	POD12_DCI	C7	DQU3	U139
AY28	DDR4_C2_DQ76	POD12_DCI	C2	DQU4	U139
BB27	DDR4_C2_DQ77	POD12_DCI	C8	DQU5	U139
BC25	DDR4_C2_DQ78	POD12_DCI	D3	DQU6	U139
BC28	DDR4_C2_DQ79	POD12_DCI	D7	DQU7	U139
BE25	DDR4_C2_DQS8_T	DIFF_POD12_DCI	G3	DQSL_C	U139
BF25	DDR4_C2_DQS8_C	DIFF_POD12_DCI	F3	DQSL_T	U139
BA26	DDR4_C2_DQS9_T	DIFF_POD12_DCI	B7	DQSU_C	U139
BB26	DDR4_C2_DQS9_C	DIFF_POD12_DCI	A7	DQSU_T	U139
BE29	DDR4_C2_DM8	POD12_DCI	E7	DML_B/DBIL_B	U139
BA29	DDR4_C2_DM9	POD12_DCI	E2	DMU_B/DBIU_B	U139
AM27	DDR4_C2_A0	SSTL12_DCI	P3	A0	U135-U139
AT25	DDR4_C2_A1	SSTL12_DCI	P7	A1	U135-U139
AN25	DDR4_C2_A2	SSTL12_DCI	R3	A2	U135-U139
AN26	DDR4_C2_A3	SSTL12_DCI	N7	A3	U135-U139
AR25	DDR4_C2_A4	SSTL12_DCI	N3	A4	U135-U139
AU28	DDR4_C2_A5	SSTL12_DCI	P8	A5	U135-U139
AU27	DDR4_C2_A6	SSTL12_DCI	P2	A6	U135-U139
AR28	DDR4_C2_A7	SSTL12_DCI	R8	A7	U135-U139
AP25	DDR4_C2_A8	SSTL12_DCI	R2	A8	U135-U139
AM26	DDR4_C2_A9	SSTL12_DCI	R7	A9	U135-U139
AP26	DDR4_C2_A10	SSTL12_DCI	M3	A10/AP	U135-U139
AN28	DDR4_C2_A11	SSTL12_DCI	T2	A11	U135-U139
AR27	DDR4_C2_A12	SSTL12_DCI	M7	A12/BC_B	U135-U139
AP28	DDR4_C2_A13	SSTL12_DCI	T8	A13	U135-U139
AU26	DDR4_C2_BA0	SSTL12_DCI	N2	BA0	U135-U139
AV26	DDR4_C2_BA1	SSTL12_DCI	N8	BA1	U135-U139
AV28	DDR4_C2_BG0	SSTL12_DCI	M2	BG0	U135-U139
AL27	DDR4_C2_A14_WE_B	SSTL12_DCI	L2	WE_B/A14	U135-U139
AP27	DDR4_C2_A15_CAS_B	SSTL12_DCI	M8	CAS_B_A15	U135-U139
AM28	DDR4_C2_A16_RAS_B	SSTL12_DCI	L8	RAS_B/A16	U135-U139
AT26	DDR4_C2_CK_T	DIFF_SSTL12_DCI	K7	CK_T	U135-U139
AT27	DDR4_C2_CK_C	DIFF_SSTL12_DCI	K8	CK_C	U135-U139
AY29	DDR4_C2_CKE	SSTL12_DCI	K2	CKE	U135-U139

Table 1-5: **DDR4 Memory 80-bit I/F C2 to FPGA U1 Banks 44, 45, and 46 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref.Des.
AW28	DDR4_C2_ACT_B	SSTL12_DCI	L3	ACT_B	U135-U139
AV25	DDR4_C2_PAR	SSTL12_DCI	P9	ALERT_B	U135-U139
BF29	DDR4_C2_ODT	SSTL12_DCI	T3	PAR	U135-U139
BB29	DDR4_C2_CS_B	SSTL12_DCI	K3	ODT	U135-U139
AW26	DDR4_C2_ALERT_B	SSTL12_DCI	L7	CS_B	U135-U139
BF40	DDR4_C2_RESET_B	LVCMOS12	P1	RESET_B	U135-U139

The VCU108 dual DDR4 80-bit memory component interfaces adhere to the constraints guidelines documented in the DDR3/DDR4 Design Guidelines section of *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (Vivado Design Suite)* (PG150) [Ref 3]. The VCU108 DDR4 memory component interface is a 40Ω impedance implementation.

For more information on the UltraScale bank internal VREF, see the "Supply Voltages for the SelectIO Pins" VREF section in *UltraScale Architecture SelectIO Resources* (UG571) [Ref 4]. For more details about the Micron DDR4 component memory, see the *Micron EDY4016AABG-DR-F-D Data Sheet* [Ref 5].

RLD3 Component Memory

[Figure 1-2, callout 5]

The 144 MB RLD3 component memory system is comprised of two 576 Mb (16M x 36) RLDRAM3 devices located at U141-U142.

- Manufacturer: Micron
- Part number: MT44K16M36RB-093E
- Configuration: 576 Mb: 1 Mb x 36 x 16 Banks
- Supply voltage: 1.35V
- Datapath width: 36 bits common I/O (CIO)
- Data rate: 1066 MHz DDR operation (2133 Mb/s/ball)

The VCU108 XCVU095 FPGA RLD3 interface performance is documented in the *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (UG893) [Ref 1].

This memory system is connected to the XCVU095 HP banks 69, 70, and 71. The RLD3 0.6V VTT termination voltage (net RLD3_C1_VTT) is sourced from TI TPS51200DR linear regulator U143. The RLD3 memory interface banks U69 – U71 VREF pins are wired to GND through 1K

resistors, invoking the INTERNAL VREF mode. The connections between the RLD3 component memories and XCVU095 banks 69, 70, and 71 are listed in Table 1-6.

Table 1-6: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 69, 70, and 71**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
A15	RLD3_C1_72B_DQ0	SSTL12	D11	DQ0	U141
B15	RLD3_C1_72B_DQ1	SSTL12	E10	DQ1	U141
A14	RLD3_C1_72B_DQ2	SSTL12	C8	DQ2	U141
C15	RLD3_C1_72B_DQ3	SSTL12	C10	DQ3	U141
A16	RLD3_C1_72B_DQ4	SSTL12	C12	DQ4	U141
B12	RLD3_C1_72B_DQ5	SSTL12	B9	DQ5	U141
C14	RLD3_C1_72B_DQ6	SSTL12	B11	DQ6	U141
A13	RLD3_C1_72B_DQ7	SSTL12	A8	DQ7	U141
B16	RLD3_C1_72B_DQ8	SSTL12	A10	DQ8	U141
C10	RLD3_C1_72B_DQ9	SSTL12	J10	DQ9	U141
A8	RLD3_C1_72B_DQ10	SSTL12	K11	DQ10	U141
B10	RLD3_C1_72B_DQ11	SSTL12	K13	DQ11	U141
A11	RLD3_C1_72B_DQ12	SSTL12	L8	DQ12	U141
B11	RLD3_C1_72B_DQ13	SSTL12	L10	DQ13	U141
A9	RLD3_C1_72B_DQ14	SSTL12	L12	DQ14	U141
C7	RLD3_C1_72B_DQ15	SSTL12	M9	DQ15	U141
B7	RLD3_C1_72B_DQ16	SSTL12	M11	DQ16	U141
B8	RLD3_C1_72B_DQ17	SSTL12	N8	DQ17	U141
F14	RLD3_C1_72B_DQ18	SSTL12	D3	DQ18	U141
H13	RLD3_C1_72B_DQ19	SSTL12	E4	DQ19	U141
E13	RLD3_C1_72B_DQ20	SSTL12	C6	DQ20	U141
F13	RLD3_C1_72B_DQ21	SSTL12	C4	DQ21	U141
E14	RLD3_C1_72B_DQ22	SSTL12	C2	DQ22	U141
G15	RLD3_C1_72B_DQ23	SSTL12	B5	DQ23	U141
G13	RLD3_C1_72B_DQ24	SSTL12	B3	DQ24	U141
H15	RLD3_C1_72B_DQ25	SSTL12	A6	DQ25	U141
F15	RLD3_C1_72B_DQ26	SSTL12	A4	DQ26	U141
G12	RLD3_C1_72B_DQ27	SSTL12	J4	DQ27	U141
D10	RLD3_C1_72B_DQ28	SSTL12	K3	DQ28	U141
H12	RLD3_C1_72B_DQ29	SSTL12	K1	DQ29	U141
F9	RLD3_C1_72B_DQ30	SSTL12	L6	DQ30	U141

Table 1-6: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 69, 70, and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
E11	RLD3_C1_72B_DQ31	SSTL12	L4	DQ31	U141
E9	RLD3_C1_72B_DQ32	SSTL12	L2	DQ32	U141
F11	RLD3_C1_72B_DQ33	SSTL12	M5	DQ33	U141
D11	RLD3_C1_72B_DQ34	SSTL12	M3	DQ34	U141
F10	RLD3_C1_72B_DQ35	SSTL12	N6	DQ35	U141
H14	RLD3_C1_72B_DM0	SSTL12	B7	DM0	U141
D7	RLD3_C1_72B_DM1	SSTL12	M7	DM1	U141
C13	RLD3_C1_72B_QK0_P	DIFF_SSTL12	D9	QK0	U141
B13	RLD3_C1_72B_QK0_N	DIFF_SSTL12	E8	QK0_B	U141
C9	RLD3_C1_72B_QK1_P	DIFF_SSTL12	K9	QK1	U141
C8	RLD3_C1_72B_QK1_N	DIFF_SSTL12	J8	QK1_B	U141
E12	RLD3_C1_72B_QK2_P	DIFF_SSTL12	D5	QK2	U141
D12	RLD3_C1_72B_QK2_N	DIFF_SSTL12	E6	QK2_B	U141
G11	RLD3_C1_72B_QK3_P	DIFF_SSTL12	K5	QK3	U141
G10	RLD3_C1_72B_QK3_N	DIFF_SSTL12	J6	QK3_B	U141
C12	RLD3_C1_72B_QVLD0	SSTL12	J12	QVLD0	U141
D15	RLD3_C1_72B_QVLD1	SSTL12	J2	QVLD1	U141
C18	RLD3_C1_72B_DQ36	SSTL12	D11	DQ0	U142
C17	RLD3_C1_72B_DQ37	SSTL12	E10	DQ1	U142
C20	RLD3_C1_72B_DQ38	SSTL12	C8	DQ2	U142
A18	RLD3_C1_72B_DQ39	SSTL12	C10	DQ3	U142
C19	RLD3_C1_72B_DQ40	SSTL12	C12	DQ4	U142
D20	RLD3_C1_72B_DQ41	SSTL12	B9	DQ5	U142
D19	RLD3_C1_72B_DQ42	SSTL12	B11	DQ6	U142
A19	RLD3_C1_72B_DQ43	SSTL12	A8	DQ7	U142
D17	RLD3_C1_72B_DQ44	SSTL12	A10	DQ8	U142
J19	RLD3_C1_72B_DQ45	SSTL12	J10	DQ9	U142
K19	RLD3_C1_72B_DQ46	SSTL12	K11	DQ10	U142
K16	RLD3_C1_72B_DQ47	SSTL12	K13	DQ11	U142
J17	RLD3_C1_72B_DQ48	SSTL12	L8	DQ12	U142
L16	RLD3_C1_72B_DQ49	SSTL12	L10	DQ13	U142
K18	RLD3_C1_72B_DQ50	SSTL12	L12	DQ14	U142
H19	RLD3_C1_72B_DQ51	SSTL12	M9	DQ15	U142
L18	RLD3_C1_72B_DQ52	SSTL12	M11	DQ16	U142

Table 1-6: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 69, 70, and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
H17	RLD3_C1_72B_DQ53	SSTL12	N8	DQ17	U142
G20	RLD3_C1_72B_DQ54	SSTL12	D3	DQ18	U142
E19	RLD3_C1_72B_DQ55	SSTL12	E4	DQ19	U142
F18	RLD3_C1_72B_DQ56	SSTL12	C6	DQ20	U142
E17	RLD3_C1_72B_DQ57	SSTL12	C4	DQ21	U142
F20	RLD3_C1_72B_DQ58	SSTL12	C2	DQ22	U142
E18	RLD3_C1_72B_DQ59	SSTL12	B5	DQ23	U142
F16	RLD3_C1_72B_DQ60	SSTL12	B3	DQ24	U142
F19	RLD3_C1_72B_DQ61	SSTL12	A6	DQ25	U142
E16	RLD3_C1_72B_DQ62	SSTL12	A4	DQ26	U142
P16	RLD3_C1_72B_DQ63	SSTL12	J4	DQ27	U142
M18	RLD3_C1_72B_DQ64	SSTL12	K3	DQ28	U142
N17	RLD3_C1_72B_DQ65	SSTL12	K1	DQ29	U142
P17	RLD3_C1_72B_DQ66	SSTL12	L6	DQ30	U142
R19	RLD3_C1_72B_DQ67	SSTL12	L4	DQ31	U142
N18	RLD3_C1_72B_DQ68	SSTL12	L2	DQ32	U142
M17	RLD3_C1_72B_DQ69	SSTL12	M5	DQ33	U142
N19	RLD3_C1_72B_DQ70	SSTL12	M3	DQ34	U142
P19	RLD3_C1_72B_DQ71	SSTL12	N6	DQ35	U142
D16	RLD3_C1_72B_DM2	SSTL12	B7	DM0	U142
H18	RLD3_C1_72B_DM3	SSTL12	M7	DM1	U142
B18	RLD3_C1_72B_QK4_P	DIFF_SSTL12	D9	QK0	U142
B17	RLD3_C1_72B_QK4_N	DIFF_SSTL12	E8	QK0_B	U142
K17	RLD3_C1_72B_QK5_P	DIFF_SSTL12	K9	QK1	U142
J16	RLD3_C1_72B_QK5_N	DIFF_SSTL12	J8	QK1_B	U142
G18	RLD3_C1_72B_QK6_P	DIFF_SSTL12	D5	QK2	U142
G17	RLD3_C1_72B_QK6_N	DIFF_SSTL12	E6	QK2_B	U142
R18	RLD3_C1_72B_QK7_P	DIFF_SSTL12	K5	QK3	U142
R17	RLD3_C1_72B_QK7_N	DIFF_SSTL12	J6	QK3_B	U142
B20	RLD3_C1_72B_QVLD2	DIFF_SSTL12	J12	QVLD0	U142
G16	RLD3_C1_72B_QVLD3	DIFF_SSTL12	J2	QVLD1	U142
J22	RLD3_C1_72B_A0	SSTL12	E2	A0	U141-U142
H22	RLD3_C1_72B_A1	SSTL12	F5	A1	U141-U142
N20	RLD3_C1_72B_A2	SSTL12	F4	A2	U141-U142

Table 1-6: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 69, 70, and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
R21	RLD3_C1_72B_A3	SSTL12	F9	A3	U141-U142
E23	RLD3_C1_72B_A4	SSTL12	F10	A4	U141-U142
J21	RLD3_C1_72B_A5	SSTL12	F12	A5	U141-U142
E22	RLD3_C1_72B_A6	SSTL12	G3	A6	U141-U142
G23	RLD3_C1_72B_A7	SSTL12	F1	A7	U141-U142
L23	RLD3_C1_72B_A8	SSTL12	G11	A8	U141-U142
K21	RLD3_C1_72B_A9	SSTL12	F13	A9	U141-U142
F21	RLD3_C1_72B_A10	SSTL12	H13	A10	U141-U142
H24	RLD3_C1_72B_A11	SSTL12	D1	A11	U141-U142
B21	RLD3_C1_72B_A12	SSTL12	H11	A12	U141-U142
K22	RLD3_C1_72B_A13	SSTL12	D13	A13	U141-U142
B23	RLD3_C1_72B_A14	SSTL12	H3	A14	U141-U142
H23	RLD3_C1_72B_A15	SSTL12	G2	A15	U141-U142
D22	RLD3_C1_72B_A16	SSTL12	H4	A16	U141-U142
M23	RLD3_C1_72B_A17	SSTL12	H10	A17	U141-U142
E21	RLD3_C1_72B_A18	SSTL12	G12	A18	U141-U142
B22	RLD3_C1_72B_A19	SSTL12	H1	NF_A19	U141-U142
N23	RLD3_C1_72B_BA0	SSTL12	G9	BA0	U141-U142
F24	RLD3_C1_72B_BA1	SSTL12	G5	BA1	U141-U142
H20	RLD3_C1_72B_BA2	SSTL12	H8	BA2	U141-U142
C22	RLD3_C1_72B_BA3	SSTL12	H6	BA3	U141-U142
F23	RLD3_C1_72B_WE_B	SSTL12	F6	WE_B	U141-U142
P20	RLD3_C1_72B_REF_B	SSTL12	F8	REF_B	U141-U142
E24	RLD3_C1_72B_CK_P	SSTL12	H7	CK	U141-U142
D24	RLD3_C1_72B_CK_N	SSTL12	G7	CK_B	U141-U142
A21	RLD3_C1_72B_RESET_B	SSTL12	A13	RESET_B	U141-U142
K23	RLD3_C1_72B_CS_B	SSTL12	E12	CS_B	U141-U142
A24	RLD3_C1_72B_DK0_P	DIFF_SSTL12	D7	DK0	U141
A23	RLD3_C1_72B_DK0_N	DIFF_SSTL12	C7	DK0_B	U141
C24	RLD3_C1_72B_DK1_P	DIFF_SSTL12	K7	DK1	U141
C23	RLD3_C1_72B_DK1_N	DIFF_SSTL12	L7	DK1_B	U141
M21	RLD3_C1_72B_DK2_P	DIFF_SSTL12	D7	DK0	U142
L21	RLD3_C1_72B_DK2_N	DIFF_SSTL12	C7	DK0_B	U142

Table 1-6: **RLD3 Memory 72-bit I/F to FPGA U1 Banks 69, 70, and 71 *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Component Memory		
			Pin#	Pin Name	Ref. Des.
M20	RLD3_C1_72B_DK3_P	DIFF_SSTL12	K7	DK1	U142
L20	RLD3_C1_72B_DK3_N	DIFF_SSTL12	L7	DK1_B	U142

The VCU108 RLD3 72-bit memory component interface adheres to the constraints guidelines documented in the RLD3 Design Guidelines section of *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (Vivado Design Suite)* (PG150) [Ref 3]. The VCU108 RLD3 memory component interface is a 40Ω impedance implementation. For more information on the UltraScale bank internal VREF, see the "Supply Voltages for the SelectIO Pins" VREF section in *UltraScale Architecture SelectIO Resources* (UG571) [Ref 4]. For more details about the Micron RLD3 component memory, see the *Micron MT44K16M36RB-093E Data Sheet* [Ref 5].

Linear BPI Flash Memory

[Figure 1-2, callout 7]

The linear BPI flash memory located at U58 provides 128 MB (1 Gbit) of nonvolatile storage that can be used for configuration or software storage. The data, address, and control signals are connected to the FPGA. The BPI flash memory device is packaged in a 64-pin BGA.

- Part number: MT28GU01GAAA1EGC-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 16 bits (26 address lines and 7 control signals)
- Data rate: up to 90 MHz

The linear BPI flash memory can synchronously configure the FPGA in master BPI mode at the 90 MHz data rate supported by the MT28GU01GAAA1EGC flash memory by using a configuration bitstream generated with BitGen options for synchronous configuration and for a configuration clock division of one. The fastest configuration method uses the external 90 MHz oscillator connected to the FPGA EMCCLK pin. By default, UltraScale FPGAs use the parallel NOR flash asynchronous read in the master BPI configuration mode.

Multiple bitstreams can be stored in the linear BPI flash memory. The two most significant address bits (A25, A24) of the flash memory are connected to DIP switch SW16 positions 1 and 2, respectively, and to the bank 65 RS1 and RS0 pins of the FPGA. By placing valid bitstreams at different offset addresses in the flash memory, various bitstreams can be selected to configure the FPGA by appropriately setting the DIP switch SW16.

VCU108 XCVU095 FPGA Bitstream Compression Required

IMPORTANT: *When four bitstreams are required, use the master BPI configuration asynchronous read mode, and specify bitstream compression.*

A full XCVU095 configuration bitstream requires 27% of the 1 Gbit linear BPI NOR flash size.

The two RS pins are tied to the upper address pins of the flash memory, which allows for easy selection of any of the four images stored in the BPI flash memory. When using this feature with the basic BPI asynchronous read mode, the bitstream sizes must be equal to or less than one fourth the size of the BPI flash device. Consequently, bitstream compression must be used with the VCU108 XCVU095 FPGAs and the 1 Gbit on-board BPI flash in this mode. At configuration boot time, the RS1 and RS0 pins are held at a static value by the SW16 settings. This allows selection of one of the four bitstreams stored in the BPI flash. The physical BPI flash address locations are defined by the static strappings of RS1 and RS0 (tied to flash A25 and A24, respectively). Refer to *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2] for more information.

Add the following constraints for compression to designs targeted for the VCU108 board.

When loading from BPI flash:

```
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type1 [current_design]
set_property CONFIG_MODE BPI16 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
```

To match the VCU108 configuration of FPGA U1 bank 0:

```
set_property CFGBVS GND [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
```

If four images are not required to be programmed, then the synchronous read mode is an option. In the master BPI configuration mode with synchronous read, the flash bursts data so it does not encounter an issue with the revision boundary (one fourth of the flash).

Figure 1-6 shows the connections of the linear BPI flash memory on the VCU108 board.

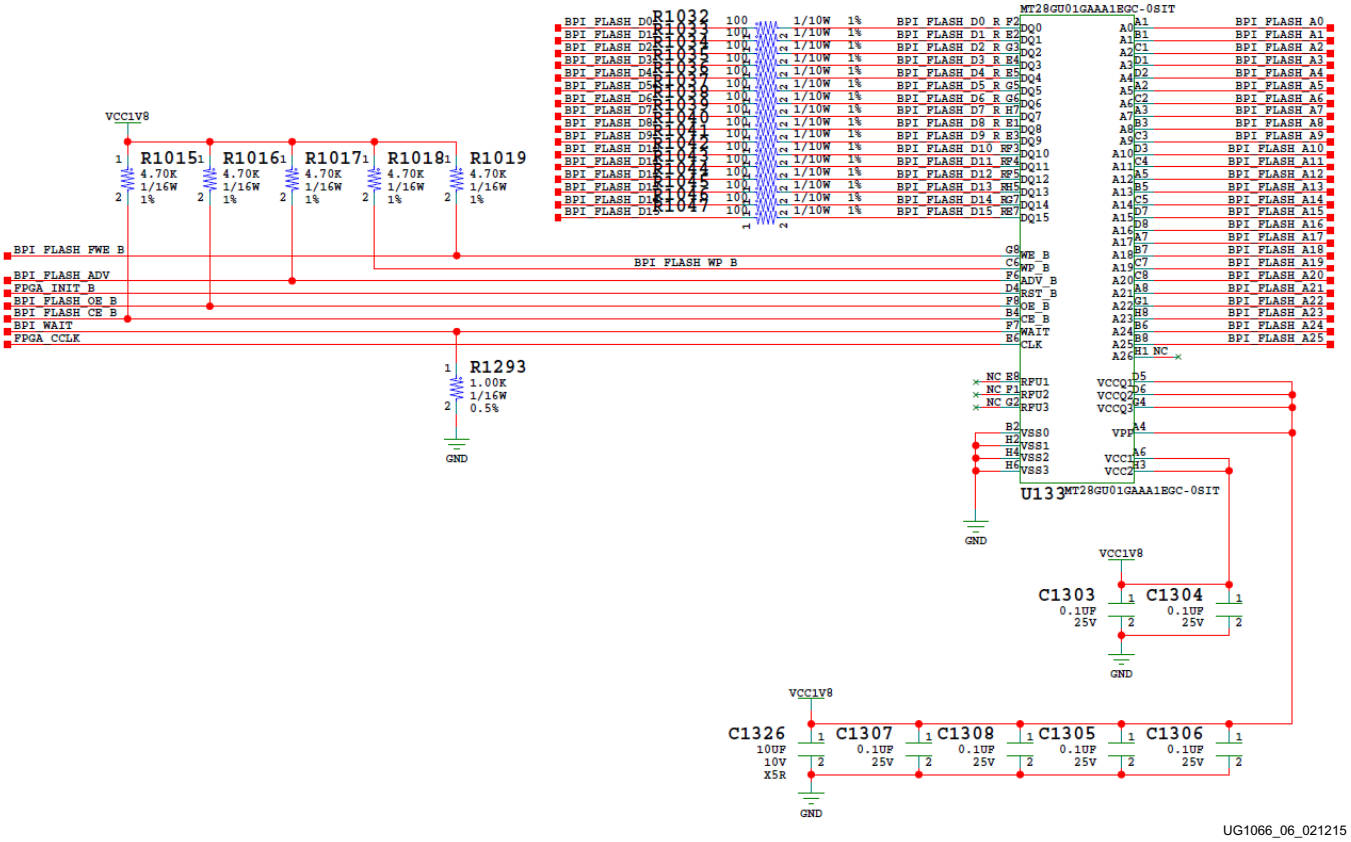


Figure 1-6: **Linear BPI 128 MB (1 Gbit) Flash Memory**

The connections between the BPI flash memory and the FPGA are listed in Table 1-7.

Table 1-7: **BPI Flash Memory Connections to FPGA U1**

FPGA (U1) Pin	Net Name	I/O Standard	U58 BPI Flash Memory	
			Pin #	Pin Name
AP11	BPI_FLASH_D0	LVCMOS18	F2	DQ0
AN11	BPI_FLASH_D1	LVCMOS18	E2	DQ1
AM11	BPI_FLASH_D2	LVCMOS18	G3	DQ2
AL11	BPI_FLASH_D3	LVCMOS18	E4	DQ3
AM19	BPI_FLASH_D4	LVCMOS18	E5	DQ4
AM18	BPI_FLASH_D5	LVCMOS18	G5	DQ5
AN20	BPI_FLASH_D6	LVCMOS18	G6	DQ6
AP20	BPI_FLASH_D7	LVCMOS18	H7	DQ7
AN19	BPI_FLASH_D8	LVCMOS18	E1	DQ8
AN18	BPI_FLASH_D9	LVCMOS18	E3	DQ9
AR18	BPI_FLASH_D10	LVCMOS18	F3	DQ10
AR17	BPI_FLASH_D11	LVCMOS18	F4	DQ11
AT20	BPI_FLASH_D12	LVCMOS18	F5	DQ12
AT19	BPI_FLASH_D13	LVCMOS18	H5	DQ13
AT17	BPI_FLASH_D14	LVCMOS18	G7	DQ14
AU17	BPI_FLASH_D15	LVCMOS18	E7	DQ15
AR20	BPI_FLASH_A0	LVCMOS18	A1	A0
AR19	BPI_FLASH_A1	LVCMOS18	B1	A1
AV20	BPI_FLASH_A2	LVCMOS18	C1	A2
AW20	BPI_FLASH_A3	LVCMOS18	D1	A3
AU19	BPI_FLASH_A4	LVCMOS18	D2	A4
AU18	BPI_FLASH_A5	LVCMOS18	A2	A5
AV19	BPI_FLASH_A6	LVCMOS18	C2	A6
AV18	BPI_FLASH_A7	LVCMOS18	A3	A7
AW18	BPI_FLASH_A8	LVCMOS18	B3	A8
AY18	BPI_FLASH_A9	LVCMOS18	C3	A9
AY19	BPI_FLASH_A10	LVCMOS18	D3	A10
BA19	BPI_FLASH_A11	LVCMOS18	C4	A11
BA17	BPI_FLASH_A12	LVCMOS18	A5	A12
BB17	BPI_FLASH_A13	LVCMOS18	B5	A13
BB19	BPI_FLASH_A14	LVCMOS18	C5	A14
BC19	BPI_FLASH_A15	LVCMOS18	D7	A15

Table 1-7: **BPI Flash Memory Connections to FPGA U1 *(Cont'd)***

FPGA (U1) Pin	Net Name	I/O Standard	U58 BPI Flash Memory	
			Pin #	Pin Name
BB18	BPI_FLASH_A16	LVCMOS18	D8	A16
BC18	BPI_FLASH_A17	LVCMOS18	A7	A17
AY20	BPI_FLASH_A18	LVCMOS18	B7	A18
BA20	BPI_FLASH_A19	LVCMOS18	C7	A19
BD18	BPI_FLASH_A20	LVCMOS18	C8	A20
BD17	BPI_FLASH_A21	LVCMOS18	A8	A21
BC20	BPI_FLASH_A22	LVCMOS18	G1	A22
BD20	BPI_FLASH_A23	LVCMOS18	H8	A23
BE20	BPI_FLASH_A24	LVCMOS18	B6	A24
BF20	BPI_FLASH_A25	LVCMOS18	B8	A25
NC	NC	NA	H1	A26
BF16	BPI_FLASH_FWE_B	LVCMOS18	G8	WE_B
P/U R1018	BPI_FLASH_WP_B	LVCMOS18	C6	WP_B
AW17	BPI_FLASH_ADV	LVCMOS18	F6	ADV_B
AC12	FPGA_INIT_B	LVCMOS18	D4	RST_B
BF17	BPI_FLASH_OE_B	LVCMOS18	F8	OE_B
AJ11	BPI_FLASH_CE_B	LVCMOS18	B4	CE_B
BC23	BPI_WAIT	LVCMOS18	F7	WAIT
AF13	FPGA_CCLK	LVCMOS18	E6	CLK

Additional FPGA bitstreams can be stored and used for configuration by setting the warm boot start address (WBSTAR) register contained in UltraScale FPGAs. More information is available in the reconfiguration and multiboot section in the *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2]. The configuration section in this document provides details on the master BPI configuration mode. For more information about the Micron MT28GU01GAAA1EGC-0SIT, see the Micron Technology website [Ref 5].

Micro-SD Card Interface

[Figure 1-2, callout 8]

The VCU108 board includes a secure digital input/output (SDIO) interface allowing the U111 XC7Z101 Zynq-7000 SoC system controller access to general purpose nonvolatile micro-SD memory cards and peripherals. The micro-SD card slot is designed to support 50 MHz high speed micro-SD cards. The SDIO signals are connected to U111 XC7Z010 Zynq-7000 SoC system controller bank 500, which has its VCCO set to SYS_1V8 1.8V. A MAX13035E level shifter is used between the micro-SD card connector (J83), the XC7Z010 system controller (U111), and the micro-SD card connector (J83). Figure 1-7 shows the connections of the SD card interface on the VCU108 board.

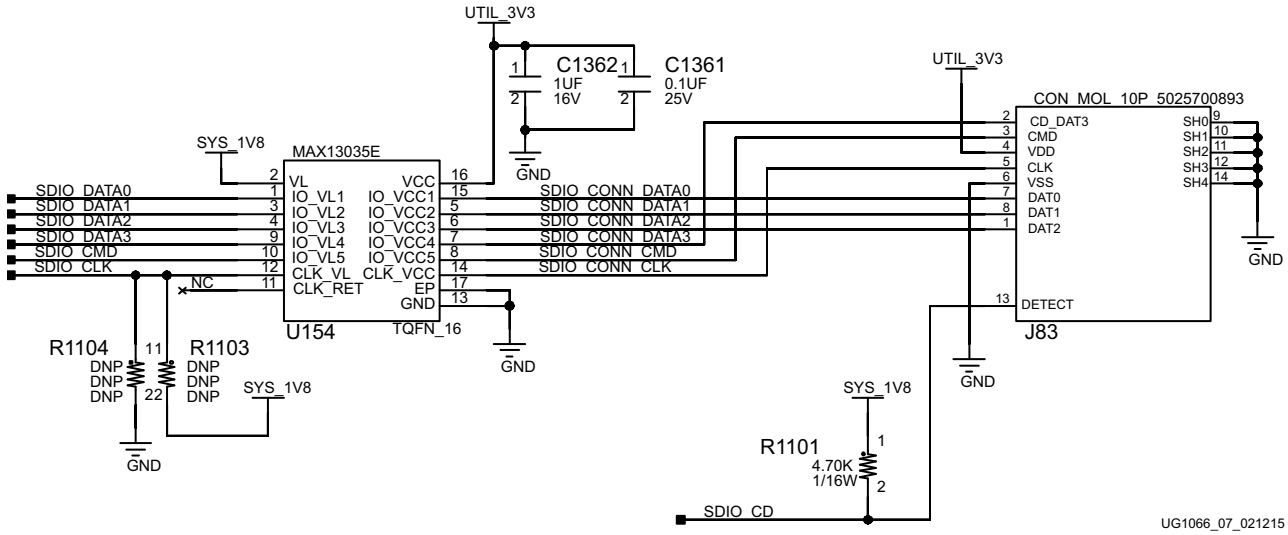


Figure 1-7: **SD Connector Circuit Topology**

The connections between the SD Card connector and System Controller U111 are listed in Table 1-8.

Table 1-8: **SD Card Connections to System Controller U111**

XC7Z010 (U111)	Schematic Net Name	I/O Standard	Level Shifter (U154)				Schematic Net Name	SDIO Connector (J83)	
			Pin #	Pin Name	Pin Name	Pin #		Pin #	Pin Name
D6	SDIO_DATA0	LVCMOS18	1	IO_VL1	IO_VCC1	15	SDIO_CONN_DATA0	7	DAT0
C6	SDIO_DATA1	LVCMOS18	3	IO_VL2	IO_VCC2	5	SDIO_CONN_DATA1	8	DAT1
B9	SDIO_DATA2	LVCMOS18	4	IO_VL3	IO_VCC3	6	SDIO_CONN_DATA2	1	DAT2
D10	SDIO_DATA3	LVCMOS18	9	IO_VL4	IOVCC4	7	SDIO_CONN_DATA3	2	CD_DAT3
B10	SDIO_CMD	LVCMOS18	10	IO_VL5	IO_VCC5	8	SDIO_CONN_CMD	3	CMD
B7	SDIO_CLK	LVCMOS18	12	CLK_VL	CLK_VCC	14	SDIO_CONN_CLK	5	CLK
D8	SDIO_CD	LVCMOS18	Direct Connect				SDIO_CD	13	DETECT

For more information on secure digital nonvolatile memory card technology, see the SanDisk [Ref 6] and SD Association [Ref 7] websites.

Digilent USB JTAG Module

[Figure 1-2, callout 9]

JTAG configuration is provided through a Digilent onboard USB-to-JTAG configuration logic module (U115) where a host computer accesses the VCU108 board JTAG chain through a type-A (host side) to micro-B (VCU108 board side J106) USB cable.

A 2 mm JTAG header (J3) is also provided in parallel for access by Xilinx download cables, such as the Platform Cable USB II. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pins M[2:0], wired to SW16 positions [3:5]. The JTAG chain of the VCU108 board is illustrated in Figure 1-8.

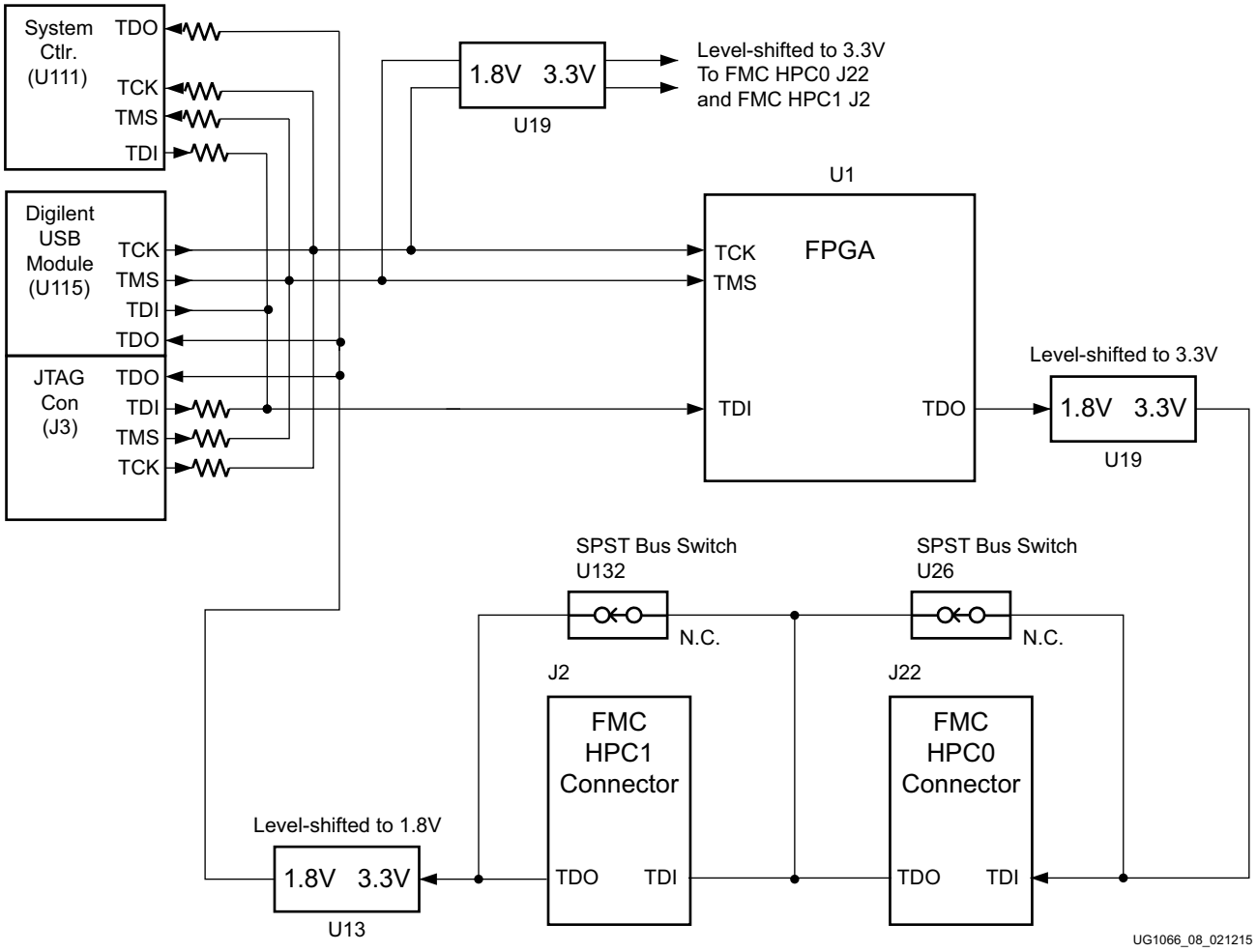


Figure 1-8: **JTAG Chain Block Diagram**

For more details about the Digilent USB JTAG Module, see the Digilent website [Ref 8].

FMC Connector JTAG Bypass

When an FMC is attached to the VCU108 board, it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switches U26 (HPC0) and U132 (HPC1). The SPST switches are in a normally closed state and transition to an open state when the FMC is attached. Switch U26 adds an attached HPC FMC to the FPGAs JTAG chain as determined by the FMC_HPC0_PRSNT_M2C_B signal. Switch U132 adds an attached HPC FMC to the FPGAs JTAG chain as determined by the FMC_HPC1_PRSNT_M2C_B signal.

IMPORTANT: *The attached FMC must implement a TDI-to-TDO connection through a device or bypass jumper to ensure that the JTAG chain connects to the FPGA U1.*

The JTAG connectivity on the VCU108 board allows a host computer to download bitstreams to the FPGA using the Xilinx tools. In addition, the JTAG connector allows debug tools such as the Vivado serial I/O analyzer or a software debugger to access the FPGA. The Xilinx tools can also program the BPI parallel flash memory.

Clock Generation

The VCU108 evaluation board provides twelve clock sources to the FPGA as listed in Table 1-9.

Table 1-9: **VCU108 Board Clock Sources**

Clock Name	Clock Reference Description	Description
System clock 300 MHz	U122/U157	Silicon Labs Si5335A 1.8V LVDS any frequency quad clock generator CLK0 drives U157 quad clock buffer. (SYSCLK1_300_P/N and SYSCLK2_300_P/N)
System clock 125 MHz	U122	Silicon Labs Si5335A 1.8V LVDS any frequency quad clock generator CLK1. (CLK_125 MHz)
EMC clock 90 MHz	U122	Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency quad clock generator CLK2. (FPGA_EMCCLK)
System control clock 33.333 MHz	U122	Silicon Labs Si5335A 1.8V LVCMOS single-ended any frequency quad clock generator CLK3. (SYSCTLR_CLK)
User clock 10 MHz-810 MHz	U32/U104	Silicon Labs Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default. U32 output Q0 drives U104 quad clock buffer. (USER_SI570_CLOCK_P/N and MGT_SI570_CLOCK1_P/N thru MGT_SI570_CLOCK3_P/N)
Jitter attenuated clock	U57	Silicon Labs Si5328B LVDS precision clock multiplier/jitter attenuator. See Jitter Attenuated Clock (SI5328_OUT1_P and SI5328_OUT1_N).

Table 1-9: **VCU108 Board Clock Sources *(Cont'd)***

Clock Name	Clock Reference Description	Description
Jitter attenuated clock	U57	Silicon Labs Si5328B LVDS precision clock multiplier/jitter attenuator. See Jitter Attenuated Clock (SI5328_OUT2_P and SI5328_OUT2_N).
User SMA clock	J34(P), J35(N)	User clock input SMAs. See User SMA Clock (USER_SMA_CLOCK_P and USER_SMA_CLOCK_N).

Table 1-10 lists the VCU108 clock sources to FPGA U1 connections.

Table 1-10: **VCU108 Clock Sources to XCVU095 FPGA U1 Connections**

Clock Source Ref. Des. and Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
U157.9	SYSCLK1_300_P	DIFF_SSTL12	G31
U157.10	SYSCLK1_300_N	DIFF_SSTL12	F31
U157.11	SYSCLK2_300_P	DIFF_SSTL12	G22
U157.12	SYSCLK2_300_N	DIFF_SSTL12	G21
U122.18	CLK_125MHZ_P	LVDS	BC9
U122.17	CLK_125MHZ_N	LVDS	BC8
U122.14	FPGA_EMCCLK(2)	LVCMOS18	AL20
U122.10	SYSCTLR_CLK(2)	LVCMOS18	U111.C7
U104.9	USER_SI570_CLOCK_P	LVDS_25	AU23
U104.10	USER_SI570_CLOCK_N	LVDS_25	AV23
U104.11	MGT_SI570_CLOCK1_P	NA(2)	V38
U104.12	MGT_SI570_CLOCK1_N	NA(2)	V39
U104.13	MGT_SI570_CLOCK2_P	NA(2)	AF38
U104.14	MGT_SI570_CLOCK2_N	NA(2)	AF39
U104.15	MGT_SI570_CLOCK3_P	NA(2)	AH38
U104.16	MGT_SI570_CLOCK3_N	NA(2)	AH39
U57.28	SI5328_OUT1_P	NA(1)	T38
U57.29	SI5328_OUT1_N	NA(1)	T39
U57.28	SI5328_OUT2_P	NA(1)	AD38
U57.29	SI5328_OUT2_N	NA(1)	AD39
J34.1	USER_SMA_CLOCK_P	LVDS	AR14
J35.1	USER_SMA_CLOCK_N	LVDS	AT14

Notes:

1. Capacitively coupled, MGT connections I/O standard is not applicable.
2. SI570 U32 SI570_OUTPUT_P/N nets are wired to quad clock buffer U104, (1) also applies.

System Clock

[Figure 1-2, callout 10]

The system clock source is a Silicon Labs SI5335A quad clock generator/buffer at U122. The system clock (SYSCLK) is a LVDS 300 MHz clock sourced from the CLK0A output pair of U122. SYSCLK is wired to a SI53340-B-GN quad clock buffer U157. The U157 Q0 signal pair named SYSCLK1_300_P/N is connected to XCVU095 FPGA U1 bank 50 global clock (GC) pins G31 and F31, respectively. The U157 Q1 signal pair named SYSCLK2_300_P/N is connected to XCVU095 FPGA U1 bank 70 global clock (GC) pins G22 and G21, respectively.

- Clock generator: Silicon Labs SI5335A-B03426-GM (CLK0A 300 MHz)
- Low phase jitter of 0.7 pS RMS
- LVDS differential output
- Quad clock buffer: Silicon Labs SI53340-B-GM (SYSCLK1, SYSCLK2 300 MHz)
- Additive phase jitter of 43 fs RMS
- LVDS differential output

The 300 MHz system clock circuit (the upper right CLK0 branch out of U122) is shown in Figure 1-9.

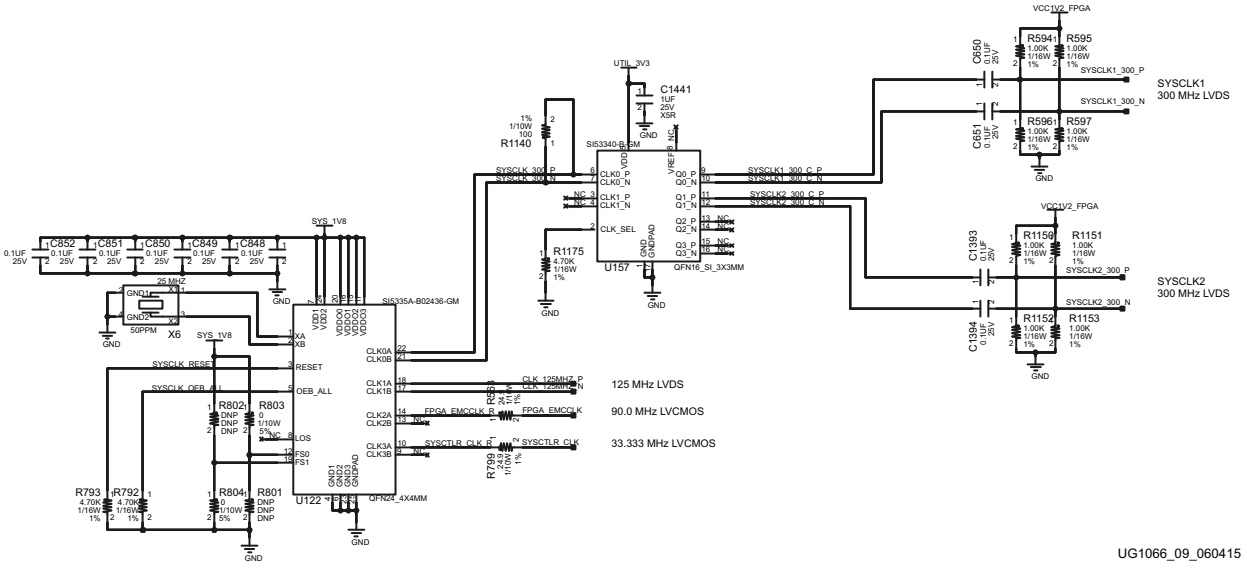


Figure 1-9: **VCU108 Board System Clock**

Three additional clocks are sourced from the U122 quad clock generator:

- 125 MHz LVDS signal pair CLK_125MHZ_P and CLK_125MHZ_N, connected to XCVU095 FPGA U1 bank 66 pins BC9 and BC8, respectively.
- 90.0 MHz single-ended 1.8V LVCMOS, series resistor coupled FPGA_EMCCLK, connected to XCVU095 FPGA U1 bank 65 dedicated EMCCLK input pin AL20.
- 33.3333 MHz single-ended 1.8V LVCMOS, series resistor coupled SYSCTLR_CLK, connected to system controller XC7Z010 Zynq-7000 SoC U111 bank 500 dedicated PS_CLK input pin C7.

Programmable User Clock

[Figure 1-2, callout 11]

The VCU108 evaluation board has a SI570 programmable low-jitter 3.3V LVDS differential oscillator (U32) connected to the CLK0 P/N inputs (pins 6 (P) and 7 (N)) of clock buffer SI53340 U104, a 3.3V 1:4 low-jitter LVDS clock buffer with 2:1 input MUX.

The 3.3V SI53340 U104 has four LVDS output clock pairs:

- U104 output Q0 drives clock pair USER_SI570_CLOCK_P/N, connected to XCVU095 FPGA U1 HR bank 84 GC pins AU23 and AV23, respectively.
- U104 output Q1 drives clock pair MGT_SI570_CLOCK1_P/N, connected to XCVU095 FPGA U1 GTY BANK 129 MGTREFCLK0P/N pins V38 and V39 (capacitively coupled), respectively.
- U104 output Q2 drives clock pair MGT_SI570_CLOCK2_P/N, connected to XCVU095 FPGA U1 GTY bank 127 MGTREFCLK0P/N pins AF38 and AF39 (capacitively coupled), respectively.
- U104 output Q3 drives clock pair MGT_SI570_CLOCK3_P/N, connected to XCVU095 FPGA U1 GTY BANK 126 MGTREFCLK1P/N pins AH38 and AH39 (capacitively coupled), respectively.

The U104 2:1 pin 2 MUX select net is pulled to GND to select the CLK0 input.

On power-up, the U32 SI570 user clock defaults to an output frequency of 156.250 MHz. The system controller and user applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the VCU108 evaluation board resets the user clock to the default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB0000544DG (10 MHz-810 MHz)
- Frequency tolerance: 50 ppm
- 3.3V LVDS differential output

The programmable clock circuit is shown in Figure 1-10.

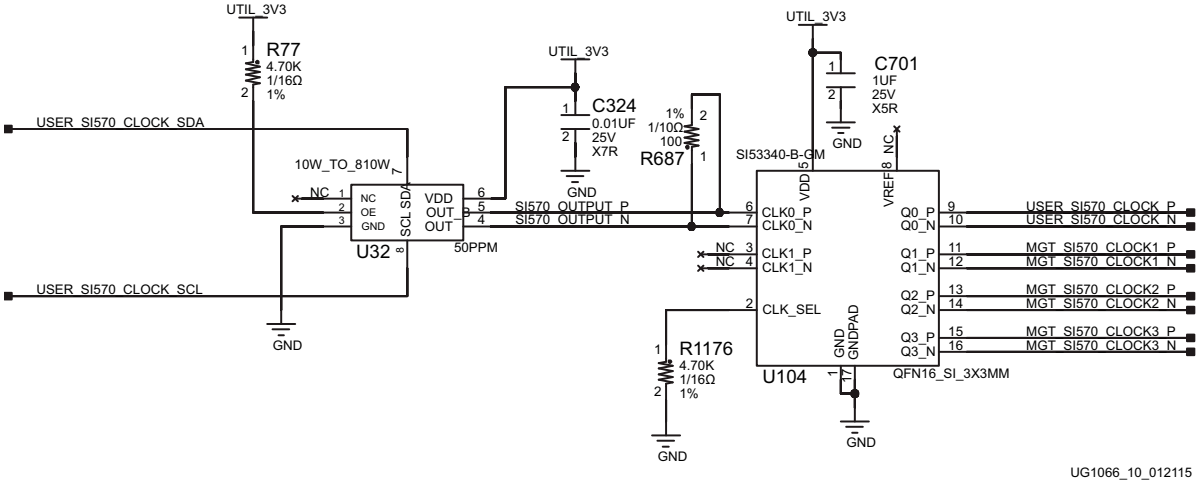


Figure 1-10: **VCU108 Board User Clock**

Jitter Attenuated Clock

[Figure 1-2, callout 12]

The VCU108 board includes a Silicon Labs Si5328B jitter attenuator U57 on the back side of the board. The FPGA U1 bank 48 can output a CFP2 RX differential clock (CFP2_RECCLK_P, pin Y32 and CFP2_RECCLK_N, pin W32) for jitter attenuation. The jitter attenuated clock (SI5328_CLOCK1_C_P (U57 pin 28), SI5328_CLOCK1_C_N (U57 pin 29)) is then routed as a reference clock to GTY Quad 129 inputs MGTREFCLK1P (U1 pin T38) and MGTREFCLK1N (U1 pin T39).

The FPGA U1 bank 47 can output a QSFP+ RX differential clock (QSFP_RECCLK_P, pin AG34 and QSFP_RECCLK_N, pin AH35) for jitter attenuation. The jitter attenuated clock (SI5328_CLOCK2_C_P (U57 pin 35), SI5328_CLOCK2_C_N (U57 pin 34)) is then routed as a reference clock to GTY Quad 127 inputs MGTREFCLK1P (U1 pin AD38) and MGTREFCLK1N (U1 pin AD39).

The primary purpose of this clock is to support synchronous protocols, such as common packet radio interface (CPRI™) or open base station architecture initiative (OBSAI). These synchronous protocols perform clock recovery from user-supplied QSFP/QSFP+ and CFP2 modules, and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTY transceiver.

The system controller configures the SI5328B in free-run mode or automatically switches over to one of two recovered clock inputs for synchronous operation (see Appendix C, System Controller). Enabling the jitter attenuation feature requires additional user programming from the FPGA through the I2C bus. The jitter attenuated clock circuit is shown in Figure 1-11.

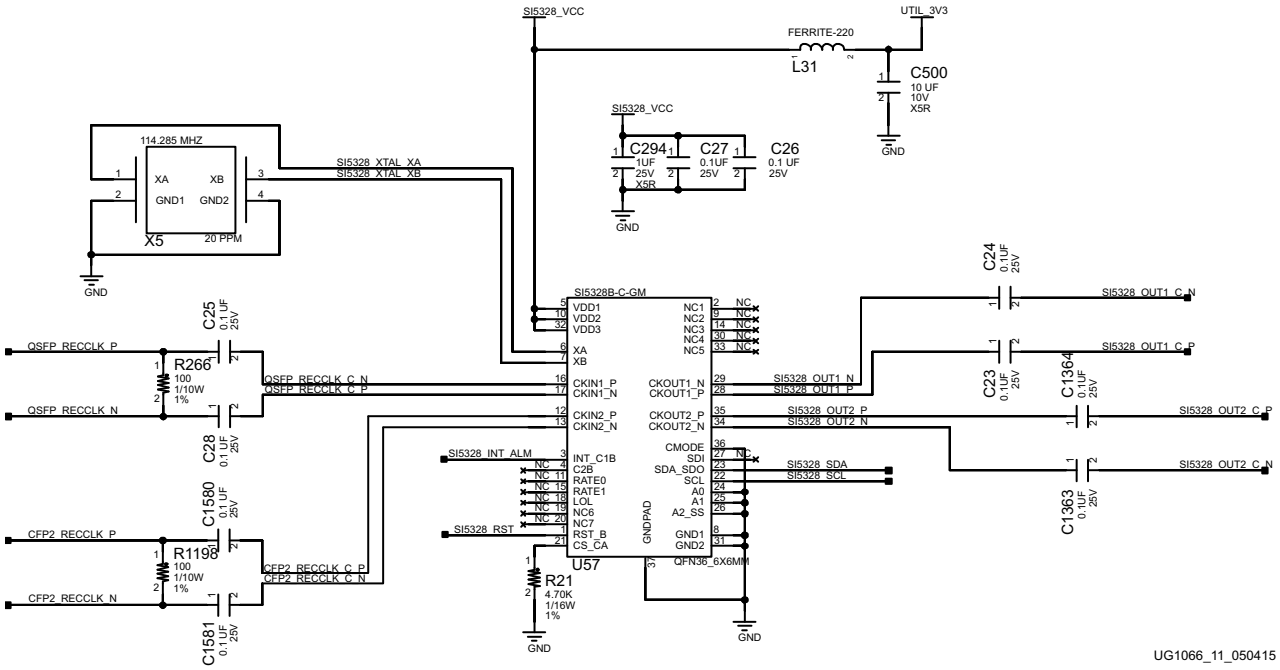


Figure 1-11: **VCU108 Board Jitter Attenuated Clock**

IMPORTANT: *The Silicon Labs Si5328 U57 pin 1 reset net SI5328_RST must be driven High to enable the device. U57 pin 1 net SI5328_RST is level-shifted to 1.8V by U48 and is connected to FPGA U1 bank 84 pin AN24.*

IMPORTANT: *The Silicon Labs Si5328 U57 component implements a 3-to-1 multiplexer. One of three input clocks (XA/B, CKIN1, or CKIN2) is selected. The selected clock drives the two clock outputs, CKOUT1 and CKOUT2, in parallel.*

An active-Low input at U57 pin 1 RST_B performs an external hardware reset of this device. This resets all internal logic to a known state and forces the device registers to their default value. The clock outputs are disabled during reset. The part must be programmed after a reset or a power-on to get a clock output. The reset pin 1 has a weak internal pull-up.

For more details on the Silicon Labs SI5335A, SI570, SI53340, and SI5328B devices, see the Silicon Labs website [Ref 9].

See *UltraScale Architecture Clocking Resources User Guide* (UG572) [Ref 10] for UltraScale FPGA clocking information.

User SMA Clock

[Figure 1-2, callout 13]

The VCU108 board provides a pair of SMAs for differential user clock input into FPGA U1 bank 67 (see Figure 1-12). The P-side SMA J34 signal USER_SMA_CLOCK_P is connected to U1 GC pin AR14, with the N-side SMA J35 signal USER_SMA_CLOCK_N connected to U1 GC pin AT14. Bank 67 VCCO is the nominally 1.8V. The USER_SMA_CLOCK input voltage swing should not exceed the voltage setting on the VADJ_1V8_FPGA rail. Any signal connected to the USER_SMA_CLOCK connector inputs must be equal to or less than the VCCO for bank 67. Valid values for the VADJ rail VADJ_1V8_FPGA are 1.5V and 1.8V. This value must be confirmed prior to applying signals to the USER_SMA_CLOCK connectors.

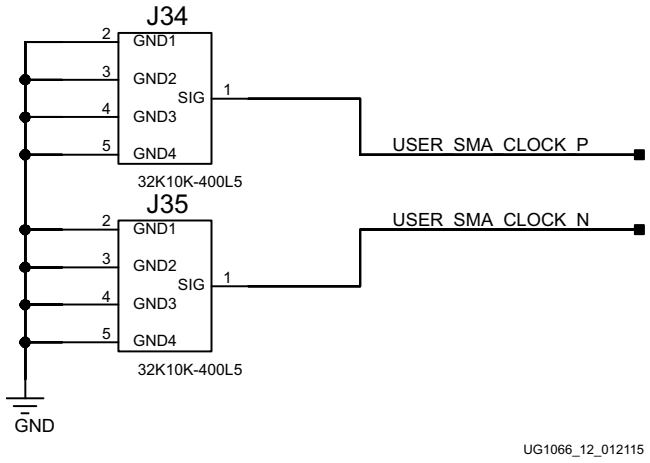


Figure 1-12: **User SMA Clock**

GTY Transceivers

[Figure 1-2, callout 2]

The VCU108 board provides access to 18 of the 24 GTY transceivers:

- Six of the GTY transceivers are not connected
- Four of the GTY transceivers are wired to a Samtec bull's eye connector (J87)
- Ten of the GTY transceivers are wired to the CFP2 connector (J89)
- Four of the GTY transceivers are wired to the QSFP module connector (U145)

The GTY transceivers in the XCVU095 are grouped into four channels described as quads. The reference clock for a quad can be sourced from the quad above or quad below the GTY quad of interest. There are six GTY quads on the VCU108 board with connectivity as listed:

Quad 125:

- MGTREFCLK0 - not connected
- MGTREFCLK1 - not connected
- Four no connect GTY transceivers

Quad 126:

- MGTREFCLK0 - BULLSEYE_GTY_REFCLK_C_P/N (J87)
- MGTREFCLK1 - MGT_SI570_CLOCK3_C_P/N (U104)
- Four GTY transceivers allocated to BULLSEYE_GTY_TX/RX[0:3]_P/N (J87)

Quad 127:

- MGTREFCLK0 - MGT_SI570_CLOCK2_C_P/N (U104)
- MGTREFCLK1 - SI5328_CLOCK2_C_P/N (U57)
- Four GTY transceivers allocated to QSFP_TX/RX[1:4]_P/N (U145)

Quad 128:

- MGTREFCLK0 - not connected)
- MGTREFCLK1 - not connected
- Four GTY transceivers allocated to CFP2_TX/RX[4,7,8,9]_P/N (J89)

Quad 129:

- MGTREFCLK0 - MGT_SI570_CLOCK1_C_P/N (U104)
- MGTREFCLK1 - SI5328_CLOCK1_C_P/N (U57)
- Four GTY transceivers allocated to CFP2_TX/RX[1,2,5,6]_P/N (J89)

Quad 130:

- MGTREFCLK0 - not connected
- MGTREFCLK1 - not connected
- Two GTY transceivers allocated to CFP2_TX/RX[0,3]_P/N (J89)
- Two GTY transceivers - not connected

Table 1-11 through Table 1-15 list the VCU108 FPGA U1 GTY transceiver bank 126-130 connections, respectively.

Table 1-11: **VCU108 FPGA U1 GTY Transceiver Bank 126 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 126	AT42	MGTYTXP0_126	BULLSEYE_GTY_TX0_P	15	P15	CCC-J-020 J87
	AT43	MGTYTXN0_126	BULLSEYE_GTY_TX0_N	16	P16	
	AR45	MGTYRXP0_126	BULLSEYE_GTY_RX0_P	17	P17	
	AR46	MGTYRXN0_126	BULLSEYE_GTY_RX0_N	18	P18	
	AP42	MGTYTXP1_126	BULLSEYE_GTY_TX1_P	13	P13	
	AP43	MGTYTXN1_126	BULLSEYE_GTY_TX1_N	14	P14	
	AN45	MGTYRXP1_126	BULLSEYE_GTY_RX1_P	11	P11	
	AN46	MGTYRXN1_126	BULLSEYE_GTY_RX1_N	12	P12	
	AM42	MGTYTXP2_126	BULLSEYE_GTY_TX2_P	7	P7	
	AM43	MGTYTXN2_126	BULLSEYE_GTY_TX2_N	8	P8	
	AL45	MGTYRXP2_126	BULLSEYE_GTY_RX2_P	9	P9	
	AL46	MGTYRXN2_126	BULLSEYE_GTY_RX2_N	10	P10	
	AL40	MGTYTXP3_126	BULLSEYE_GTY_TX3_P	5	P5	
	AL41	MGTYTXN3_126	BULLSEYE_GTY_TX3_N	6	P6	
	AJ45	MGTYRXP3_126	BULLSEYE_GTY_RX3_P	3	P3	
	AJ46	MGTYRXN3_126	BULLSEYE_GTY_RX3_N	4	P4	
	AK38	MGTREFCLK0P_126	BULLSEYE_GTY_REFCLK_C_P	19	P19	
	AK39	MGTREFCLK0N_126	BULLSEYE_GTY_REFCLK_C_N	20	P20	
	AH38	MGTREFCLK1P_126	MGT_SI570_CLOCK3_C_P	15	Q3_P	Si570 U32 through clock buffer U104
	AH39	MGTREFCLK1N_126	MGT_SI570_CLOCK3_C_N	16	Q3_N	

Table 1-12: **VCU108 FPGA U1 GTY Transceiver Bank 127 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 127	AK42	MGTYTXP0_127	QSFP_TX1_P	36	TX1P	QSFP+ FS1-R38-20A2-10 U145
	AK43	MGTYTXN0_127	QSFP_TX1_N	37	TX1N	
	AG45	MGTYRXP0_127	QSFP_RX1_P	17	RX1P	
	AG46	MGTYRXN0_127	QSFP_RX1_N	18	RX1N	
	AJ40	MGTYTXP1_127	QSFP_TX2_P	3	TX2P	
	AJ41	MGTYTXN1_127	QSFP_TX2_N	2	TX2N	
	AF43	MGTYRXP1_127	QSFP_RX2_P	22	RX2P	
	AF44	MGTYRXN1_127	QSFP_RX2_N	21	RX2N	
	AG40	MGTYTXP2_127	QSFP_TX3_P	33	TX3P	
	AG41	MGTYTXN2_127	QSFP_TX3_N	34	TX3N	
	AE45	MGTYRXP2_127	QSFP_RX3_P	14	RX3P	
	AE46	MGTYRXN2_127	QSFP_RX3_N	15	RX3N	
	AE40	MGTYTXP3_127	QSFP_TX4_P	6	TX4P	
	AE41	MGTYTXN3_127	QSFP_TX4_N	5	TX4N	
	AD43	MGTYRXP3_127	QSFP_RX4_P	25	RX4P	
	AD44	MGTYRXN3_127	QSFP_RX4_N	24	RX4N	
	AF38	MGTREFCLK0P_127	MGT_SI570_CLOCK2_C_P	13	Q2_P	Si570 U32 through clock buffer U104
	AF39	MGTREFCLK0N_127	MGT_SI570_CLOCK2_C_N	14	Q2_N	
	AD38	MGTREFCLK1P_127	SI5328_CLOCK2_C_P	35	CKOUT2_P	SI5328-B-GM U57
	AD39	MGTREFCLK1N_127	SI5328_CLOCK2_C_N	34	CKOUT2_N	

For additional information about the quad small form factor pluggable (28 Gb/s QSFP+) module, see the SFF-8663 specification for the 28 Gb/s QSFP+ at the SFF-8663 specification website [Ref 11].

Table 1-13: **VCU108 FPGA U1 GTY Transceiver Bank 128 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 128	AC40	MGTYTXP0_128	CFP2_TX9_X_P	3	TX9_P	CFP2 J89
	AC41	MGTYTXN0_128	CFP2_TX9_X_N	2	TX9_N	
	AC45	MGTYRXP0_128	CFP2_RX9_X_P	48	RX9_P	
	AC46	MGTYRXN0_128	CFP2_RX9_X_N	47	RX9_N	
	AA40	MGTYTXP1_128	CFP2_TX8_X_P	6	TX8_P	
	AA41	MGTYTXN1_128	CFP2_TX8_X_N	5	TX8_N	
	AB43	MGTYRXP1_128	CFP2_RX8_X_P	51	RX8_P	
	AB44	MGTYRXN1_128	CFP2_RX8_X_N	50	RX8_N	
	W40	MGTYTXP2_128	CFP2_TX7_X_P	102	TX7_P	
	W41	MGTYTXN2_128	CFP2_TX7_X_N	103	TX7_N	
	AA45	MGTYRXP2_128	CFP2_RX7_X_P	75	RX7_P	
	AA46	MGTYRXN2_128	CFP2_RX7_X_N	76	RX7_N	
	U40	MGTYTXP3_128	CFP2_TX4_X_P	93	TX4_P	
	U41	MGTYTXN3_128	CFP2_TX4_X_N	94	TX4_N	
	Y43	MGTYRXP3_128	CFP2_RX4_X_P	66	RX4_P	
	Y44	MGTYRXN3_128	CFP2_RX4_X_N	67	RX4_N	
	AB38	MGTREFCLK0P_128	NC	NA	NA	NA
	AB39	MGTREFCLK0N_128	NC	NA	NA	
	Y38	MGTREFCLK1P_128	NC	NA	NA	NA
	Y39	MGTREFCLK1N_128	NC	NA	NA	

The CFP2 interface supports two 100 Gb/s modes; 10 channels x 10 Gb/s and 4 channels by 25 Gb/s. For additional information about the 100 Gb/s small form factor pluggable (CFP2) module, see the CFP MSA CFP2 hardware specification website [Ref 12].

Table 1-14: **VCU108 FPGA U1 GTY Transceiver Bank 129 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 129	T42	MGTYTXP0_129	CFP2_TX6_3_P	99	TX6_P	CFP2 J89
	T43	MGTYTXN0_129	CFP2_TX6_3_N	100	TX6_N	
	W45	MGTYRXP0_129	CFP2_RX6_3_P	72	RX6_P	
	W46	MGTYRXN0_129	CFP2_RX6_3_N	73	RX6_N	
	P42	MGTYTXP1_129	CFP2_TX5_2_P	96	TX5_P	
	P43	MGTYTXN1_129	CFP2_TX5_2_N	97	TX5_N	
	U45	MGTYRXP1_129	CFP2_RX5_2_P	69	RX5_P	
	U46	MGTYRXN1_129	CFP2_RX5_2_N	70	RX5_N	
	M42	MGTYTXP2_129	CFP2_TX2_1_P	87	TX2_P	
	M43	MGTYTXN2_129	CFP2_TX2_1_N	88	TX2_N	
	R45	MGTYRXP2_129	CFP2_RX2_1_P	60	RX2_P	
	R46	MGTYRXN2_129	CFP2_RX2_1_N	61	RX2_N	
	K42	MGTYTXP3_129	CFP2_TX1_0_P	84	TX1_P	
	K43	MGTYTXN3_129	CFP2_TX1_0_N	85	TX1_N	
	N45	MGTYRXP3_129	CFP2_RX1_0_P	57	RX1_P	
	N46	MGTYRXN3_129	CFP2_RX1_0_N	58	RX1_N	
	V38	MGTREFCLK0P_129	MGT_SI570_CLOCK1_C_P	11	Q1_P	Si570 U32 through clock buffer U104
	V39	MGTREFCLK0N_129	MGT_SI570_CLOCK1_C_N	12	Q1_N	
	T38	MGTREFCLK1P_129	SI5328_CLOCK1_C_P	28	CKOUT1_P	SI5328-B-GM U57
	T39	MGTREFCLK1N_129	SI5328_CLOCK1_C_N	29	CKOUT1_N	

Table 1-15: **VCU108 FPGA U1 GTY Transceiver Bank 130 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTY Bank 130	H42	MGTYTXP0_130	CFP2_TX3_X_P	90	TX3_P	CFP2 J89
	H43	MGTYTXN0_130	CFP2_TX3_X_N	91	TX3_N	
	L45	MGTYRXP0_130	CFP2_RX3_X_P	63	RX3_P	
	L46	MGTYRXN0_130	CFP2_RX3_X_N	64	RX3_N	
	F42	MGTYTXP1_130	CFP2_TX0_X_P	81	TX0_P	
	F43	MGTYTXN1_130	CFP2_TX0_X_N	82	TX0_N	
	J45	MGTYRXP1_130	CFP2_RX0_X_P	54	RX0_P	
	J46	MGTYRXN1_130	CFP2_RX0_X_N	55	RX0_N	
	D42	MGTYTXP2_130	NC	NA	NA	
	D43	MGTYTXN2_130	NC	NA	NA	NA
	G45	MGTYRXP2_130	NC	NA	NA	
	G46	MGTYRXN2_130	NC	NA	NA	
	B42	MGTYTXP3_130	NC	NA	NA	
	B43	MGTYTXN3_130	NC	NA	NA	
	E45	MGTYRXP3_130	NC	NA	NA	
	E46	MGTYRXN3_130	NC	NA	NA	
	R40	MGTREFCLK0P_130	NC	NA	NA	NA
	R41	MGTREFCLK0N_130	NC	NA	NA	
	N40	MGTREFCLK1P_130	NC	NA	NA	NA
	N41	MGTREFCLK1N_130	NC	NA	NA	

For additional information on GTY transceivers, see *UltraScale Architecture GTY Transceivers User Guide* (UG578) [Ref 13]. Also see *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182) [Ref 14].

GTH Transceivers

[Figure 1-2, callout 3]

The VCU108 board provides access to 28 GTH transceivers:

- Eight of the GTH transceivers are wired to the PCI Express x8 edge connector (P1)
- Ten of the GTH transceivers are wired to the FMC HPC0 connector (J22)
- Ten of the GTH transceivers are wired to the FMC HPC1 connector (J2)

The GTH transceivers in the XCVU095 are grouped into four channels described as quads. The reference clock for a quad can be sourced from the quad above or quad below the GTH quad of interest. There are seven GTH quads on the VCU108 board with connectivity as listed:

Quad 224:

- MGTREFCLK0 - not connected
- MGTREFCLK1 - not connected
- Contains four GTH transceivers allocated to PCIe lanes 7-4

Quad 225:

- MGTREFCLK0 - PCIE_CLK_Q0_P/N PCIe edge connector clock (P1)
- MGTREFCLK1 - not connected
- Contains four GTH transceivers allocated to PCIe lanes 3-0

Quad 226:

- MGTREFCLK0 - not connected
- MGTREFCLK1 - not connected
- Contains four GTH transceivers allocated to FMC_HPC1_DP[0:3] (J2)

Quad 227:

- MGTREFCLK0 - FMC_HPC1_GBTCLK0_M2C_C_P/N clock (J2)
- MGTREFCLK1 - FMC_HPC1_GBTCLK1_M2C_C_P/N clock (J2)
- Contains four GTH transceivers allocated to FMC_HPC1_DP[4:7] (J2)

Quad 228:

- MGTREFCLK0 - BULLSEYE_GTH_REFCLK_P/N (J87)
- MGTREFCLK1 - not connected
- Contains two GTH transceivers allocated to FMC_HPC0_DP[8:9] (J22)
- Contains two GTH transceivers allocated to FMC_HPC1_DP[8:9] (J2)

Quad 229:

- MGTREFCLK0 - FMC_HPC0_GBTCLK0_M2C_C_P/N clock (J22)
- MGTREFCLK1 - FMC_HPC0_GBTCLK1_M2C_C_P/N clock (J22)
- Contains four GTH transceivers allocated to FMC_HPC0_DP[4:7] (J22)

Quad 230:

- MGTREFCLK0 - not connected
- MGTREFCLK1 - not connected
- Contains four GTH transceivers allocated to FMC_HPC0_DP[0:3] (J22)

For additional information on GTH transceivers, see *UltraScale Architecture GTH Transceivers User Guide* (UG576) [Ref 15] and *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182) [Ref 14].

Table 1-16 through Table 1-22 below list the VCU108 FPGA U1 GTH Bank 224-230 connections, respectively.

Table 1-16: **VCU108 FPGA U1 GTH Bank 224 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTH Bank 224	BE5	MGTHTXP0_224	PCIE_TX7_P	A47	PERp7	PCIe EDGE P1
	BE4	MGTHTXN0_224	PCIE_TX7_N	A48	PERn7	
	BB2	MGTHRXP0_224	PCIE_RX7_P	B45	PETp7	
	BB1	MGTHRXN0_224	PCIE_RX7_N	B46	PETn7	
	BC5	MGTHTXP1_224	PCIE_TX6_P	A43	PERp6	
	BC4	MGTHTXN1_224	PCIE_TX6_N	A44	PERn6	
	AY2	MGTHRXP1_224	PCIE_RX6_P	B41	PETp6	
	AY1	MGTHRXN1_224	PCIE_RX6_N	B42	PETn6	
	BA5	MGTHTXP2_224	PCIE_TX5_P	A39	PERp5	
	BA4	MGTHTXN2_224	PCIE_TX5_N	A40	PERn5	
	AV2	MGTHRXP2_224	PCIE_RX5_P	B37	PETp5	
	AV1	MGTHRXN2_224	PCIE_RX5_N	B38	PETn5	
	AW5	MGTHTXP3_224	PCIE_TX4_P	A35	PERp4	
	AW4	MGTHTXN3_224	PCIE_TX4_N	A36	PERn4	
	AT2	MGTHRXP3_224	PCIE_RX4_P	B33	PETp4	
	AT1	MGTHRXN3_224	PCIE_RX4_N	B34	PETn4	
	AR9	MGTREFCLK0P_224	NC	NA	NA	NA
	AR8	MGTREFCLK0N_224	NC	NA	NA	
	AN9	MGTREFCLK1P_224	NC	NA	NA	NA
	AN8	MGTREFCLK1N_224	NC	NA	NA	

Table 1-17: **VCU108 FPGA U1 GTH Bank 225 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTH Bank 225	AU5	MGTHTXP0_225	PCIE_TX3_P	A29	PERp3	PCIe EDGE P1
	AU4	MGTHTXN0_225	PCIE_TX3_N	A30	PERn3	
	AP2	MGTHRXP0_225	PCIE_RX3_P	B27	PETp3	
	AP1	MGTHRXN0_225	PCIE_RX3_N	B28	PETn3	
	AT7	MGTHTXP1_225	PCIE_TX2_P	A25	PERp2	
	AT6	MGTHTXN1_225	PCIE_TX2_N	A26	PERn2	
	AM2	MGTHRXP1_225	PCIE_RX2_P	B23	PETp2	
	AM1	MGTHRXN1_225	PCIE_RX2_N	B24	PETn2	
	AR5	MGTHTXP2_225	PCIE_TX1_P	A21	PERp1	
	AR4	MGTHTXN2_225	PCIE_TX1_N	A22	PERn1	
	AK2	MGTHRXP2_225	PCIE_RX1_P	B19	PETp1	
	AK1	MGTHRXN2_225	PCIE_RX1_N	B20	PETn1	
	AP7	MGTHTXP3_225	PCIE_TX0_P	A16	PERp0	
	AP6	MGTHTXN3_225	PCIE_TX0_N	A17	PERn0	
	AJ4	MGTHRXP3_225	PCIE_RX0_P	B14	PETp0	
	AJ3	MGTHRXN3_225	PCIE_RX0_N	B15	PETn0	
	AL9	MGTREFCLK0P_225	PCIE_CLK_Q0_P	A13	REFCLK+	
	AL8	MGTREFCLK0N_225	PCIE_CLK_Q0_N	A14	REFCLK-	
	AJ9	MGTREFCLK1P_225	NC	NA	NA	NA
	AJ8	MGTREFCLK1N_225	NC	NA	NA	

Table 1-18: **VCU108 FPGA U1 GTH Bank 226 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTH Bank 226	AN5	MGTHTXP0_226	FMC_HPC1_DP0_C2M_P	C2	DP0_C2M_P	FMC HPC1 J2
	AN4	MGTHTXN0_226	FMC_HPC1_DP0_C2M_N	C3	DP0_C2M_N	
	AH2	MGTHRXP0_226	FMC_HPC1_DP0_M2C_P	C6	DP0_M2C_P	
	AH1	MGTHRXN0_226	FMC_HPC1_DP0_M2C_N	C7	DP0_M2C_N	
	AM7	MGTHTXP1_226	FMC_HPC1_DP1_C2M_P	A22	DP1_C2M_P	
	AM6	MGTHTXN1_226	FMC_HPC1_DP1_C2M_N	A23	DP1_C2M_N	
	AG4	MGTHRXP1_226	FMC_HPC1_DP1_M2C_P	A2	DP1_M2C_P	
	AG3	MGTHRXN1_226	FMC_HPC1_DP1_M2C_N	A3	DP1_M2C_N	
	AK7	MGTHTXP2_226	FMC_HPC1_DP2_C2M_P	A26	DP2_C2M_P	
	AK6	MGTHTXN2_226	FMC_HPC1_DP2_C2M_N	A27	DP2_C2M_N	
	AF2	MGTHRXP2_226	FMC_HPC1_DP2_M2C_P	A6	DP2_M2C_P	
	AF1	MGTHRXN2_226	FMC_HPC1_DP2_M2C_N	A7	DP2_M2C_N	
	AH7	MGTHTXP3_226	FMC_HPC1_DP3_C2M_P	A30	DP3_C2M_P	
	AH6	MGTHTXN3_226	FMC_HPC1_DP3_C2M_N	A31	DP3_C2M_N	
	AE4	MGTHRXP3_226	FMC_HPC1_DP3_M2C_P	A10	DP3_M2C_P	
	AE3	MGTHRXN3_226	FMC_HPC1_DP3_M2C_N	A11	DP3_M2C_N	
	AG9	MGTREFCLK0P_226	NC	NA	NA	NA
	AG8	MGTREFCLK0N_226	NC	NA	NA	
	AE9	MGTREFCLK1P_226	NC	NA	NA	NA
	AE8	MGTREFCLK1N_226	NC	NA	NA	

Table 1-19: **VCU108 FPGA U1 GTH Bank 227 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTH Bank 227	AF7	MGTHTXP0_227	FMC_HPC1_DP4_C2M_P	A34	DP4_C2M_P	FMC HPC1 J2
	AF6	MGTHTXN0_227	FMC_HPC1_DP4_C2M_N	A35	DP4_C2M_N	
	AD2	MGTHRXP0_227	FMC_HPC1_DP4_M2C_P	A14	DP4_M2C_P	
	AD1	MGTHRXN0_227	FMC_HPC1_DP4_M2C_N	A15	DP4_M2C_N	
	AD7	MGTHTXP1_227	FMC_HPC1_DP5_C2M_P	A38	DP5_C2M_P	
	AD6	MGTHTXN1_227	FMC_HPC1_DP5_C2M_N	A39	DP5_C2M_N	
	AC4	MGTHRXP1_227	FMC_HPC1_DP5_M2C_P	A18	DP5_M2C_P	
	AC3	MGTHRXN1_227	FMC_HPC1_DP5_M2C_N	A19	DP5_M2C_N	
	AB7	MGTHTXP2_227	FMC_HPC1_DP6_C2M_P	B36	DP6_C2M_P	
	AB6	MGTHTXN2_227	FMC_HPC1_DP6_C2M_N	B37	DP6_C2M_N	
	AB2	MGTHRXP2_227	FMC_HPC1_DP6_M2C_P	B16	DP6_M2C_P	
	AB1	MGTHRXN2_227	FMC_HPC1_DP6_M2C_N	B17	DP6_M2C_N	
	Y7	MGTHTXP3_227	FMC_HPC1_DP7_C2M_P	B32	DP7_C2M_P	
	Y6	MGTHTXN3_227	FMC_HPC1_DP7_C2M_N	B33	DP7_C2M_N	
	AA4	MGTHRXP3_227	FMC_HPC1_DP7_M2C_P	B12	DP7_M2C_P	
	AA3	MGTHRXN3_227	FMC_HPC1_DP7_M2C_N	B13	DP7_M2C_N	
	AC9	MGTREFCLK0P_227	FMC_HPC1_GBTCLK0_M2C_C_P	D4	GBTCLK0_M2C_P	
	AC8	MGTREFCLK0N_227	FMC_HPC1_GBTCLK0_M2C_C_N	D5	GBTCLK0_M2C_N	
	AA9	MGTREFCLK1P_227	FMC_HPC1_GBTCLK1_M2C_C_P	B20	GBTCLK1_M2C_P	
	AA8	MGTREFCLK1N_227	FMC_HPC1_GBTCLK1_M2C_C_N	B21	GBTCLK1_M2C_N	

Table 1-20: **VCU108 FPGA U1 GTH Bank 228 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTH Bank 228	V7	MGTHTXP0_228	FMC_HPC0_DP8_C2M_P	B28	DP8_C2M_P	FMC HPC0 J22
	V6	MGTHTXN0_228	FMC_HPC0_DP8_C2M_N	B29	DP8_C2M_N	
	Y2	MGTHRXP0_228	FMC_HPC0_DP8_M2C_P	B8	DP8_M2C_P	
	Y1	MGTHRXN0_228	FMC_HPC0_DP8_M2C_N	B9	DP8_M2C_N	
	T7	MGTHTXP1_228	FMC_HPC0_DP9_C2M_P	B24	DP9_C2M_P	
	T6	MGTHTXN1_228	FMC_HPC0_DP9_C2M_N	B25	DP9_C2M_N	
	W4	MGTHRXP1_228	FMC_HPC0_DP9_M2C_P	B4	DP9_M2C_P	
	W3	MGTHRXN1_228	FMC_HPC0_DP9_M2C_N	B5	DP9_M2C_N	
	P7	MGTHTXP2_228	FMC_HPC1_DP8_C2M_P	B28	DP8_C2M_P	FMC HPC1 J2
	P6	MGTHTXN2_228	FMC_HPC1_DP8_C2M_N	B29	DP8_C2M_N	
	V2	MGTHRXP2_228	FMC_HPC1_DP8_M2C_P	B8	DP8_M2C_P	
	V1	MGTHRXN2_228	FMC_HPC1_DP8_M2C_N	B9	DP8_M2C_N	
	M7	MGTHTXP3_228	FMC_HPC1_DP9_C2M_P	B24	DP9_C2M_P	
	M6	MGTHTXN3_228	FMC_HPC1_DP9_C2M_N	B25	DP9_C2M_N	
	U4	MGTHRXP3_228	FMC_HPC1_DP9_M2C_P	B4	DP9_M2C_P	
	U3	MGTHRXN3_228	FMC_HPC1_DP9_M2C_N	B5	DP9_M2C_N	
	W9	MGTREFCLK0P_228	BULLSEYE_GTH_REFCLK_C_P	1	P1	CCC-J-020 J87
	W8	MGTREFCLK0N_228	BULLSEYE_GTH_REFCLK_C_N	2	P2	
	U9	MGTREFCLK1P_228	NC	NA	NA	NA
	U8	MGTREFCLK1N_228	NC	NA	NA	

Table 1-21: **VCU108 FPGA U1 GTH Bank 229 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTH Bank 229	L5	MGTHTXP0_229	FMC_HPC0_DP4_C2M_P	A34	DP4_C2M_P	FMC HPC0 J22
	L4	MGTHTXN0_229	FMC_HPC0_DP4_C2M_N	A35	DP4_C2M_N	
	T2	MGTHRXP0_229	FMC_HPC0_DP4_M2C_P	A14	DP4_M2C_P	
	T1	MGTHRXN0_229	FMC_HPC0_DP4_M2C_N	A15	DP4_M2C_N	
	K7	MGTHTXP1_229	FMC_HPC0_DP5_C2M_P	A38	DP5_C2M_P	
	K6	MGTHTXN1_229	FMC_HPC0_DP5_C2M_N	A39	DP5_C2M_N	
	R4	MGTHRXP1_229	FMC_HPC0_DP5_M2C_P	A18	DP5_M2C_P	
	R3	MGTHRXN1_229	FMC_HPC0_DP5_M2C_N	A19	DP5_M2C_N	
	J5	MGTHTXP2_229	FMC_HPC0_DP6_C2M_P	B36	DP6_C2M_P	
	J4	MGTHTXN2_229	FMC_HPC0_DP6_C2M_N	B37	DP6_C2M_N	
	P2	MGTHRXP2_229	FMC_HPC0_DP6_M2C_P	B16	DP6_M2C_P	
	P1	MGTHRXN2_229	FMC_HPC0_DP6_M2C_N	B17	DP6_M2C_N	
	H7	MGTHTXP3_229	FMC_HPC0_DP7_C2M_P	B32	DP7_C2M_P	
	H6	MGTHTXN3_229	FMC_HPC0_DP7_C2M_N	B33	DP7_C2M_N	
	M2	MGTHRXP3_229	FMC_HPC0_DP7_M2C_P	B12	DP7_M2C_P	
	M1	MGTHRXN3_229	FMC_HPC0_DP7_M2C_N	B13	DP7_M2C_N	
	R9	MGTREFCLK0P_229	FMC_HPC0_GBTCLK0_M2C_C_P	D4	GBTCLK0_M2C_P	
	R8	MGTREFCLK0N_229	FMC_HPC0_GBTCLK0_M2C_C_N	D5	GBTCLK0_M2C_N	
	N9	MGTREFCLK1P_229	FMC_HPC0_GBTCLK1_M2C_C_N	B20	GBTCLK1_M2C_P	
	N8	MGTREFCLK1N_229	FMC_HPC0_GBTCLK1_M2C_C_P	B21	GBTCLK1_M2C_N	

Table 1-22: **VCU108 FPGA U1 GTH Bank 230 Connections**

MGT Bank	FPGA (U1) Pin	FPGA (U1) Pin Name	Schematic Net Name	Connected Pin	Connected Pin Name	Connected Device
GTH Bank 230	G5	MGTHTXP0_230	FMC_HPC0_DP0_C2M_P	C2	DP0_C2M_P	FMC HPC0 J22
	G4	MGTHTXN0_230	FMC_HPC0_DP0_C2M_N	C3	DP0_C2M_N	
	K2	MGTHRXP0_230	FMC_HPC0_DP0_M2C_P	C6	DP0_M2C_P	
	K1	MGTHRXN0_230	FMC_HPC0_DP0_M2C_N	C7	DP0_M2C_N	
	F7	MGTHTXP1_230	FMC_HPC0_DP1_C2M_P	A22	DP1_C2M_P	
	F6	MGTHTXN1_230	FMC_HPC0_DP1_C2M_N	A23	DP1_C2M_N	
	H2	MGTHRXP1_230	FMC_HPC0_DP1_M2C_P	A2	DP1_M2C_P	
	H1	MGTHRXN1_230	FMC_HPC0_DP1_M2C_N	A3	DP1_M2C_N	
	E5	MGTHTXP2_230	FMC_HPC0_DP2_C2M_P	A26	DP2_C2M_P	
	E4	MGTHTXN2_230	FMC_HPC0_DP2_C2M_N	A27	DP2_C2M_N	
	F2	MGTHRXP2_230	FMC_HPC0_DP2_M2C_P	A6	DP2_M2C_P	
	F1	MGTHRXN2_230	FMC_HPC0_DP2_M2C_N	A7	DP2_M2C_N	
	C5	MGTHTXP3_230	FMC_HPC0_DP3_C2M_P	A30	DP3_C2M_P	
	C4	MGTHTXN3_230	FMC_HPC0_DP3_C2M_N	A31	DP3_C2M_N	
	D2	MGTHRXP3_230	FMC_HPC0_DP3_M2C_P	A10	DP3_M2C_P	
	D1	MGTHRXN3_230	FMC_HPC0_DP3_M2C_N	A11	DP3_M2C_N	
	L9	MGTREFCLK0P_230	NC	NA	NA	NA
	L8	MGTREFCLK0N_230	NC	NA	NA	
	J9	MGTREFCLK1P_230	NC	NA	NA	NA
	J8	MGTREFCLK1N_230	NC	NA	NA	

PCI Express Endpoint Connectivity

[Figure 1-2, callout 14]

The 8-lane PCI Express edge connector P1 is capable of data transfers at the rate of 2.5 GT/s for Gen1 applications, 5.0 GT/s for Gen2 applications, and 8.0 GT/s for Gen3 applications. The PCIe transmit and receive signal datapaths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair.

The XCVU095-2FFVA2104E (–2 speed grade) is deployed on the VCU108 to support up to Gen3 x8.

The PCIe reference clock input is from the P1 edge connector. It is AC coupled to FPGA U1 through the MGTREFCLK0 pins of Quad 225. PCIE_CLK_Q0_P is connected to U1 pin AL9, and the _N net is connected to pin AL8. The PCI Express clock circuit is shown in Figure 1-13.

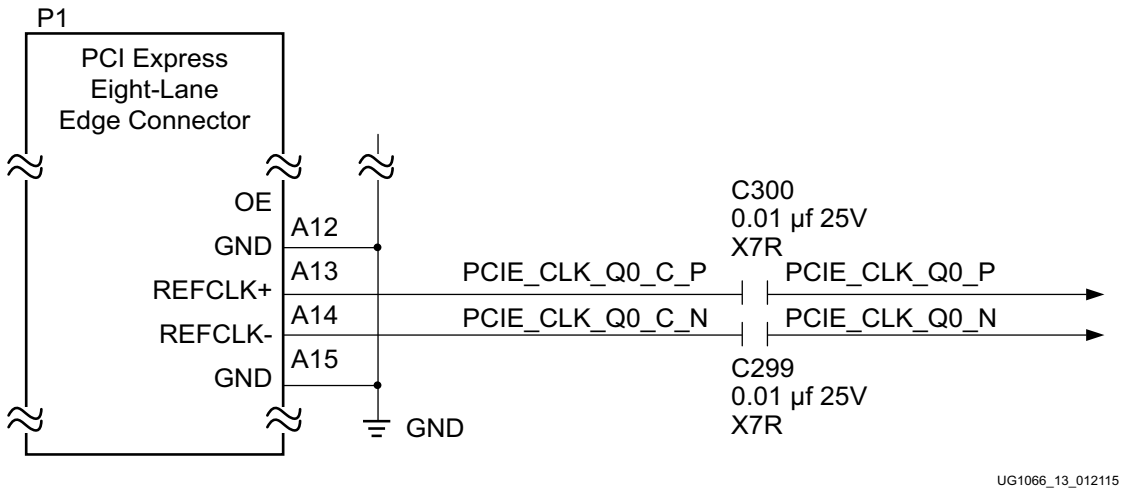


Figure 1-13: **PCI Express Clock**

PCIe lane width/size is selected by jumper J74 (Figure 1-14). The default lane size selection is 8-lane (J74 pins 5 and 6 jumpered).

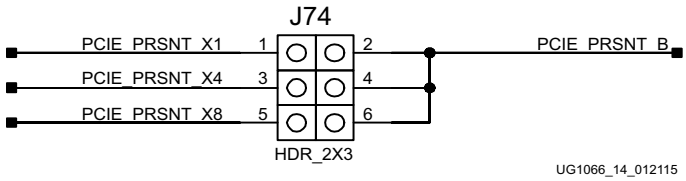


Figure 1-14: **PCI Express Lane Size Select Jumper J74**

Table 1-23 details the PCIe P1 edge connector wiring to FPGA U1.

Table 1-23: **VCU108 Board FPGA U1 to PCIe Edge P1 Connections**

FPGA (U1) Pin	Schematic Net Name	PCIe Edge P1	
		Pin Number	Pin Name
BE5	PCIE_TX7_P	A47	PERp7
BE4	PCIE_TX7_N	A48	PERn7
BB2	PCIE_RX7_P	B45	PETp7
BB1	PCIE_RX7_N	B46	PETn7
BC5	PCIE_TX6_P	A43	PERp6
BC4	PCIE_TX6_N	A44	PERn6
AY2	PCIE_RX6_P	B41	PETp6
AY1	PCIE_RX6_N	B42	PETn6
BA5	PCIE_TX5_P	A39	PERp5
BA4	PCIE_TX5_N	A40	PERn5
AV2	PCIE_RX5_P	B37	PETp5
AV1	PCIE_RX5_N	B38	PETn5
AW5	PCIE_TX4_P	A35	PERp4
AW4	PCIE_TX4_N	A36	PERn4
AT2	PCIE_RX4_P	B33	PETp4
AT1	PCIE_RX4_N	B34	PETn4
AU5	PCIE_TX3_P	A29	PERp3
AU4	PCIE_TX3_N	A30	PERn3
AP2	PCIE_RX3_P	B27	PETp3
AP1	PCIE_RX3_N	B28	PETn3
AT7	PCIE_TX2_P	A25	PERp2
AT6	PCIE_TX2_N	A26	PERn2
AM2	PCIE_RX2_P	B23	PETp2
AM1	PCIE_RX2_N	B24	PETn2
AR5	PCIE_TX1_P	A21	PERp1
AR4	PCIE_TX1_N	A22	PERn1
AK2	PCIE_RX1_P	B19	PETp1
AK1	PCIE_RX1_N	B20	PETn1
AP7	PCIE_TX0_P	A16	PERp0
AP6	PCIE_TX0_N	A17	PERn0
AJ4	PCIE_RX0_P	B14	PETp0
AJ3	PCIE_RX0_N	B15	PETn0

Table 1-23: **VCU108 Board FPGA U1 to PCIe Edge P1 Connections *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	PCIe Edge P1	
		Pin Number	Pin Name
AL9	PCIE_CLK_QO_P	A13	REFCLK+
AL8	PCIE_CLK_QO_N	A14	REFCLK-

For additional information about UltraScale PCIe functionality, see *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156) [Ref 16]. Additional information about the PCI Express standard is available at the PCI Express® standard website [Ref 17].

28 Gb/s QSFP+ Module Connector

[Figure 1-2, callout 15]

The VCU108 board contains a quad (4-channel) small form-factor pluggable (28 Gb/s QSFP+) connector U145 that accepts 28 Gb/s QSFP+ optical modules. The connector is housed within a single 28 Gb/s QSFP+ cage assembly. Figure 1-15 shows the 28 Gb/s QSFP+ module connector circuitry.

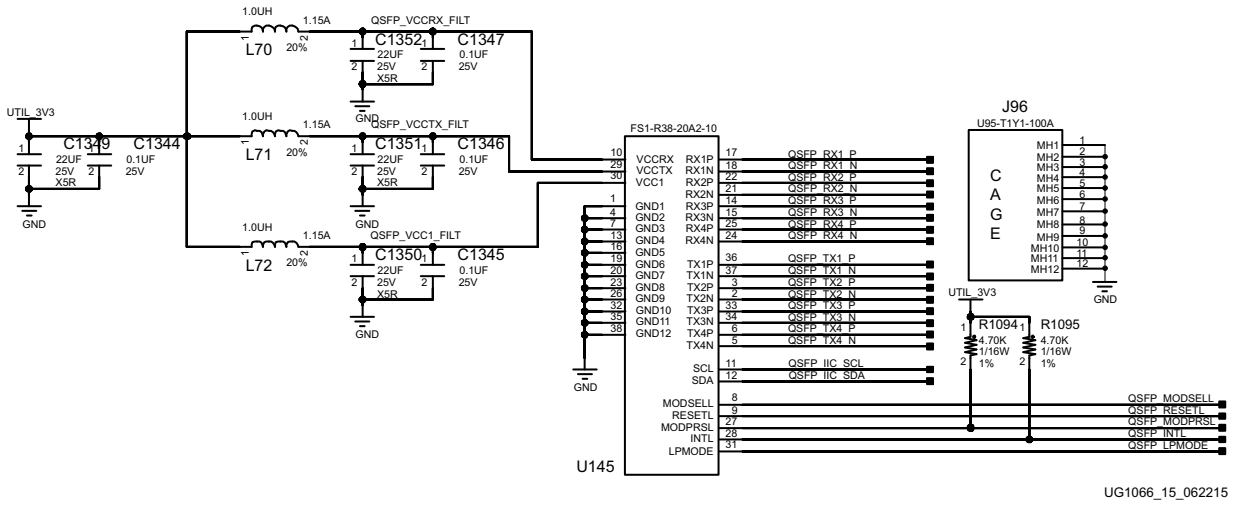


Figure 1-15: **28 Gb/s QSFP+ Module Connector**

The connections between the 28 Gb/s QSFP+ module connector U145 and the FPGA are listed in Table 1-24.

Table 1-24: **VCU108 Board FPGA U1 to QSFP+ Module Connections**

FPGA (U1) Pin	Schematic Net Name	FPGA (U1) Direction	QSFP+ Pin Number	QSFP+ Pin Name
AG45	QSFP_RX1_P	Input	17	RX1P
AG46	QSFP_RX1_N	Input	18	RX1N
AF43	QSFP_RX2_P	Input	22	RX2P
AF44	QSFP_RX2_N	Input	21	RX2N
AE45	QSFP_RX3_P	Input	14	RX3P
AE46	QSFP_RX3_N	Input	15	RX3N
AD43	QSFP_RX4_P	Input	25	RX4P
AD44	QSFP_RX4_N	Input	24	RX4N
AK42	QSFP_TX1_P	Output	36	TX1P
AK43	QSFP_TX1_N	Output	37	TX1N
AJ40	QSFP_TX2_P	Output	3	TX2P
AJ41	QSFP_TX2_N	Output	2	TX2N
AG40	QSFP_TX3_P	Output	33	TX3P
AG41	QSFP_TX3_N	Output	34	TX3N
AE41	QSFP_TX4_P	Output	6	TX4P
AD43	QSFP_TX4_N	Output	5	TX4N
U28.5	QSFP_IIC_SCL(1)	Output	11	SCL
U28.4	QSFP_IIC_SDA(1)	BiDir	12	SDA
AL24	QSFP_MODSELL(2)	Output	8	MODSELL
AM24	QSFP_RESETL(2)	Output	9	RESETL
AL25	QSFP_MODPRSL(2)	Output	27	MODPRSL
AL21	QSFP_INTL(2)	Input	28	INTL
AM21	QSFP_LPMODE(2)	Output	31	LPMODE

Notes:

1. The QSFP+ connectors U145 I2C SCL/SDA are connected to the I2C switch U28 to the IIC_MAIN_SCL/SDA bus. See I2C Bus, Topology, and Switches.
2. The QSFP+ connector U145 I2C control signals are level-shifted by U152.

   For additional information about the quad small form factor pluggable (28 Gb/s QSFP+) module, see the SFF-8663 specification for the 28 Gb/s QSFP+ at the SFF-8663 specification website [Ref 11].

CFP2 Module Connector

[Figure 1-2, callout 16]

The VCU108 board contains a 100 Gb/s form-factor pluggable (CFP) connector J89 that accepts a CFP2 optical module. The connector is housed within a single CFP2 cage assembly. Figure 1-16 shows the CFP2 module connector circuitry.

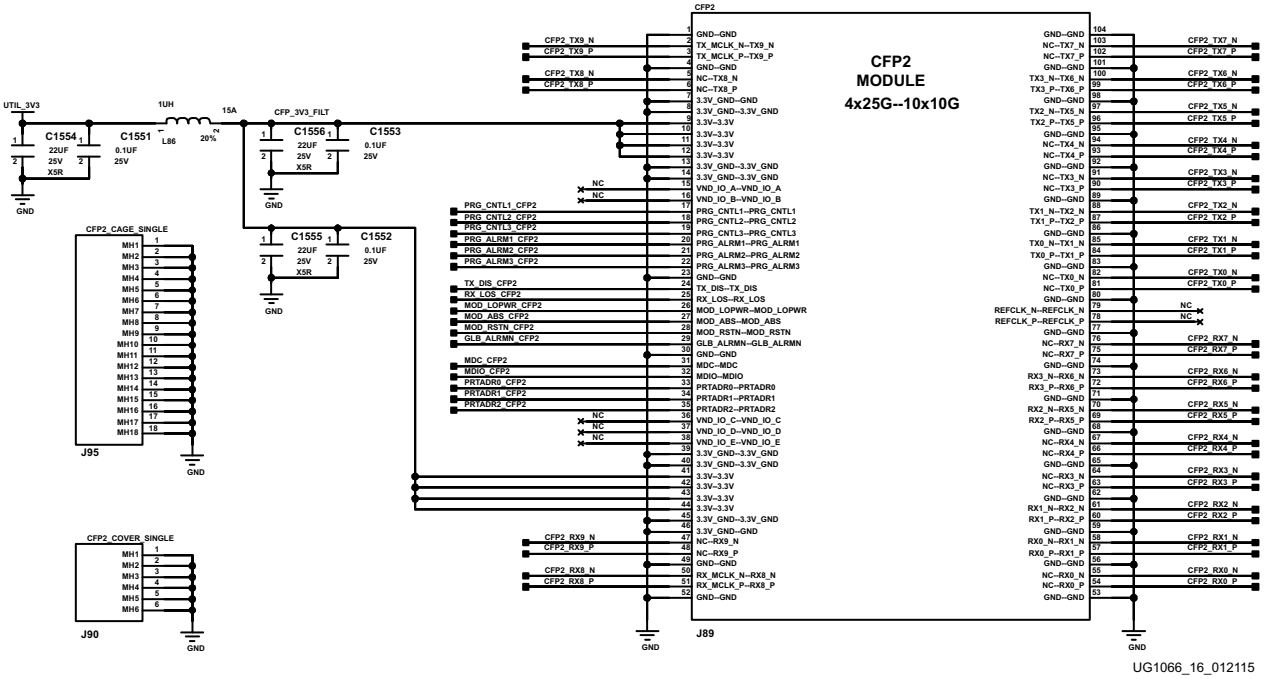


Figure 1-16: **CFP2 Module Connector**

The CFP2 can support either 4x25G or 10x10G interfaces. For details on identifying 10x10G and 4x25G pin usage, see the CFP2 hardware specification document on the CFP multi-source agreement (MSA) website [Ref 12] under the Documents tab. The CFP2 Electrical Connectors Pin Assignment section shows pin-map tables for CFP2 N x 25 Gbit/s and CFP2 10 x 10 Gbit/s.

The connections between the CFP2 module connector J89 and the FPGA are listed in Table 1-25.

Table 1-25: **VCU108 Board FPGA U1 to CFP2 Module Connections**

FPGA (U1) Pin	Schematic Net Name	FPGA (U1) Direction	CFP2 Pin Number	CFP2 Pin Name
AC40	CFP2_TX9_X_P	Output	3	TX9_P
AC41	CFP2_TX9_X_N	Output	2	TX9_N
AA40	CFP2_TX8_X_P	Output	6	TX8_P
AA41	CFP2_TX8_X_N	Output	5	TX8_N
W40	CFP2_TX7_X_P	Output	102	TX7_P
W41	CFP2_TX7_X_N	Output	103	TX7_N
T42	CFP2_TX6_3_P	Output	99	TX6_P
T43	CFP2_TX6_3_N	Output	100	TX6_N
P42	CFP2_TX5_2_P	Output	96	TX5_P
P43	CFP2_TX5_2_N	Output	97	TX5_N
U40	CFP2_TX4_X_P	Output	93	TX4_P
U41	CFP2_TX4_X_N	Output	94	TX4_N
H42	CFP2_TX3_X_P	Output	90	TX3_P
H43	CFP2_TX3_X_N	Output	91	TX3_N
M42	CFP2_TX2_1_P	Output	87	TX2_P
M43	CFP2_TX2_1_N	Output	88	TX2_N
K42	CFP2_TX1_0_P	Output	84	TX1_P
K43	CFP2_TX1_0_N	Output	85	TX1_N
F42	CFP2_TX0_X_P	Output	81	TX0_P
F43	CFP2_TX0_X_N	Output	82	TX0_N
AC45	CFP2_RX9_X_P	Input	48	RX9_P
AC46	CFP2_RX9_X_N	Input	47	RX9_N
AB43	CFP2_RX8_X_P	Input	51	RX8_P
AB44	CFP2_RX8_X_N	Input	50	RX8_N
AA45	CFP2_RX7_X_P	Input	75	RX7_P
AA46	CFP2_RX7_X_N	Input	76	RX7_N
W45	CFP2_RX6_3_P	Input	72	RX6_P
W46	CFP2_RX6_3_N	Input	73	RX6_N
U45	CFP2_RX5_2_P	Input	69	RX5_P
U46	CFP2_RX5_2_N	Input	70	RX5_N
Y43	CFP2_RX4_X_P	Input	66	RX4_P
Y44	CFP2_RX4_X_N	Input	67	RX4_N

Table 1-25: **VCU108 Board FPGA U1 to CFP2 Module Connections *(Cont'd)***

FPGA (U1) Pin	Schematic Net Name	FPGA (U1) Direction	CFP2 Pin Number	CFP2 Pin Name
L45	CFP2_RX3_X_P	Input	63	RX3_P
L46	CFP2_RX3_X_N	Input	64	RX3_N
R45	CFP2_RX2_1_P	Input	60	RX2_P
R46	CFP2_RX2_1_N	Input	61	RX2_N
N45	CFP2_RX1_0_P	Input	57	RX1_P
N46	CFP2_RX1_0_N	Input	58	RX1_N
J45	CFP2_RX0_X_P	Input	54	RX0_P
J46	CFP2_RX0_X_N	Input	55	RX0_N
BA21	PRG_CNTL1_CFP2	Output	17	PRG_CNTL1
AY24	PRG_CNTL2_CFP2	Output	18	PRG_CNTL2
AY23	PRG_CNTL3_CFP2	Output	19	PRG_CNTL3
BB24	PRG_ALRM1_CFP2	Input	20	PRG_ALRM1
BB23	PRG_ALRM2_CFP2	Input	21	PRG_ALRM2
BB22	PRG_ALRM3_CFP2	Input	22	PRG_ALRM3
BA22	PRTADR0_CFP2	Output	33	PRTADR0
AW25	PRTADR1_CFP2	Output	34	PRTADR1
AY25	PRTADR2_CFP2	Output	35	PRTADR2
AY22	TX_DIS_CFP2	Output	24	TX_DIS
BB21	RX_LOS_CFP2	Input	25	RX_LOS
BC21	MOD_LOPWR_CFP2	Output	26	MOD_LOPWR
BD21	MOD_RSTN_CFP2	Output	27	MOD_RSTN
BA25	MOD_ABS_CFP2	Input	28	MOD_ABS
BA24	GLB_ALRMN_CFP2	Input	29	GLB_ALRMN
BE22	MDC_CFP2	Output	31	MDC
BF22	MDIO_CFP2	Bidirectional	32	MDIO

Notes:

The CFP2 control nets are level-shifted by U144, U146, U147, U148, and U149. The CFP2 management interface supports IEEE 802.3 Clause 45 MDIO frames.

For additional information about the 100 Gb/s small form factor pluggable (CFP2) module, see the CFP MSA CFP2 hardware specification website [Ref 12].

10/100/1000 Mb/s Tri-Speed Ethernet PHY

[Figure 1-2, callout 17]

The VCU108 evaluation board uses the Marvell Alaska PHY device (M88E1111) at U58 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1000 Mb/s. The board supports SGMII mode only. The PHY connection to a user-provided Ethernet cable is through RJ-45 connector P3, a Halo HFJ11-1G01E-L12RL with built-in magnetics and status LEDs.

On power-up, or on reset, the PHY is configured to operate in SGMII mode with PHY address `0b00111` using the settings shown in Table 1-26. These settings can be overwritten using software commands passed over the MDIO interface.

Table 1-26: **Board Connections for PHY Configuration Pins**

Pin	Bit[2]	Bit[1]	Bit[0]	Default Values for Bit[2:0]	Setting Description
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr `00111`. Do not advertise the PAUSE bit.
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 MHz CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	100	SGMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	110	
CFG6	SEL_BDT	INT_POL	75/50Ω	010	MDC/MDIO selected. Active-Low interrupt. 50Ω SERDES option.

Table 1-27 details the FPGA U1 to U58 M88E111 Ethernet PHY connections.

Table 1-27: **FPGA U1 to Ethernet PHY U58 Connections**

FPGA (U1) Pin	Net Name	I/O Standard	M88E1111 PHY U58	
			Pin	Name
AV24	PHY_MDIO	LVCMOS18	M1	MDIO_SDA
AV21	PHY_MDC	LVCMOS18	L3	MDC_SCL
AT21	PHY_INT	LVCMOS18	L1	INT_B
AU21	PHY_RESET	LVCMOS18	K3	RESET_B

Notes:
1. Ethernet PHY_ U58 signals are level-shifted to 1.8V for interface to FPGA U1 bank 84.

Ethernet PHY Status LEDs

[Figure 1-2, callout 18]

The Ethernet PHY status LEDs are integrated into the metal frame of the P3 RJ-45 connector. These LEDs are visible on the left edge of the VCU108 board when it is installed into a PCIe slot in a PC chassis. The two PHY status LEDs are integrated within the frame of the RJ45 Ethernet jack as shown in Figure 1-17.

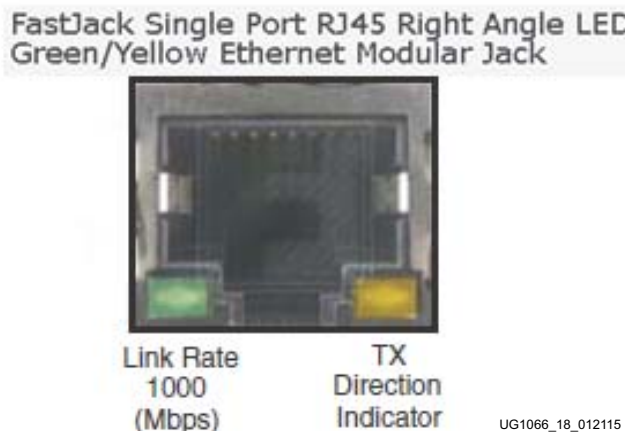


Figure 1-17: **Ethernet PHY Status LEDs**

Details about the tri-mode Ethernet MAC core are provided in *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051) [Ref 18].

The product brief for the Marvell 88E1111 Alaska Gigabit Ethernet Transceiver can be found at the Marvell website [Ref 19]. The data sheet can be obtained under NDA with Marvell. Contact information is at the Marvell website.

Dual USB-to-UART Bridge

[Figure 1-2, callout 19]

The VCU108 evaluation board contains a Silicon Labs CP2105GM dual USB-to-UART bridge device (U34) that allows a connection to a host computer with a USB port. The USB cable is supplied in the VCU108 evaluation kit (standard type-A end to host computer, type micro-B end to VCU108 evaluation board connector J4). The CP2105GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the VCU108 evaluation board.

The dual UART interface connections are split between two components:

- UART1 SCI 4-wire interface is connected to the XCVU095 U1 FPGA
- UART2 ECI 2-wire interface is connected to the XC7Z010 U111 Zynq-7000 SoC system controller

Table 1-28 lists the dual-UART U34 connections to FPGA U1.

Silicon Labs provides royalty-free virtual COM port (VCP) drivers for the host computer. These drivers permit the CP2105GM dual USB-to-UART bridge to appear as a pair of COM ports to communications application software (for example, Tera Term or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the VCU108 evaluation board. The driver assigns the lower PC COM port number to UART2 and the higher PC COM port number to UART1. See System Controller Menu in Appendix C steps 1 and 2 for VCP driver installation instructions.

The Silicon Labs CP2105GM dual USB-to-UART bridge circuit is shown in Figure 1-18.

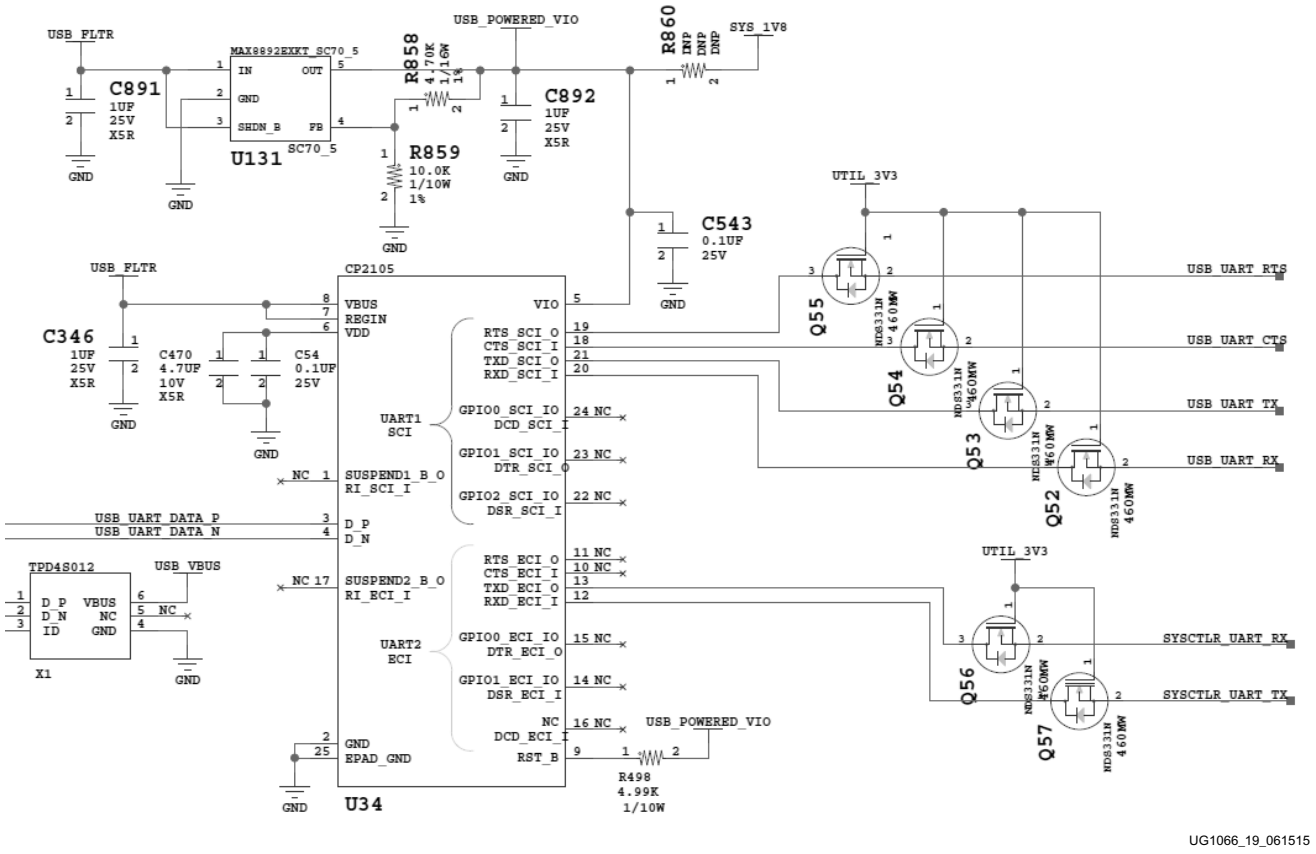


Figure 1-18: **VCU108 Dual UART CP2105GM U34**

The USB connector pin assignments and signal definitions between J4 and U34 are listed in Table 1-28.

Table 1-28: **FPGA U1 to CP2105GM U34 Connections**

FPGA (U1) Pin	Function	Direction	I/O Standard	Schematic Net Name	CP2105GM Device (U34)		
					Pin	Function	Direction
XCVU095 FPGA (U1) – UART1 SCI[1]							
BC24	RX	Input	LVCMOS18	USB_UART_TX	21	TXD	Output
BE24	TX	Output	LVCMOS18	USB_UART_RX	20	RXD	Input
BF24	CTS	Output	LVCMOS18	USB_UART_CTS	18	CTS	Input
BD22	RTS	Input	LVCMOS18	USB_UART_RTS	19	RTS	Output

Notes:
1. The USB_UART_sig nets are named from the perspective of the CP2105GM device (U34).

For more technical information on the CP2105GM and the VCP drivers, see the Silicon Labs website [Ref 9].

Xilinx UART IP is expected to be implemented in the FPGA logic using IP. See the *AXI UART Lite LogiCORE IP Product Guide* (PG142) [Ref 20] for more information.

HDMI Video Output

[Figure 1-2, callout 20]

The VCU108 evaluation board includes an HDMI video output using an Analog Devices ADV7511KSTZ-P HDMI transmitter at U52. The HDMI transmitter U52 is connected to XCVU095 FPGA banks 47 and 48 and its output is a Molex 538-47151-001 HDMI type-A receptacle at P6. The ADV7511 supports 1080P 60 Hz, YCbCr 4:2:2 encoding using 16-bit input data mapping.

The VCU108 evaluation board supports these HDMI device interfaces:

- 16 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt out pin to FPGA
- I2C
- SPDIF

The HDMI U52 circuit is shown in Figure 1-19.

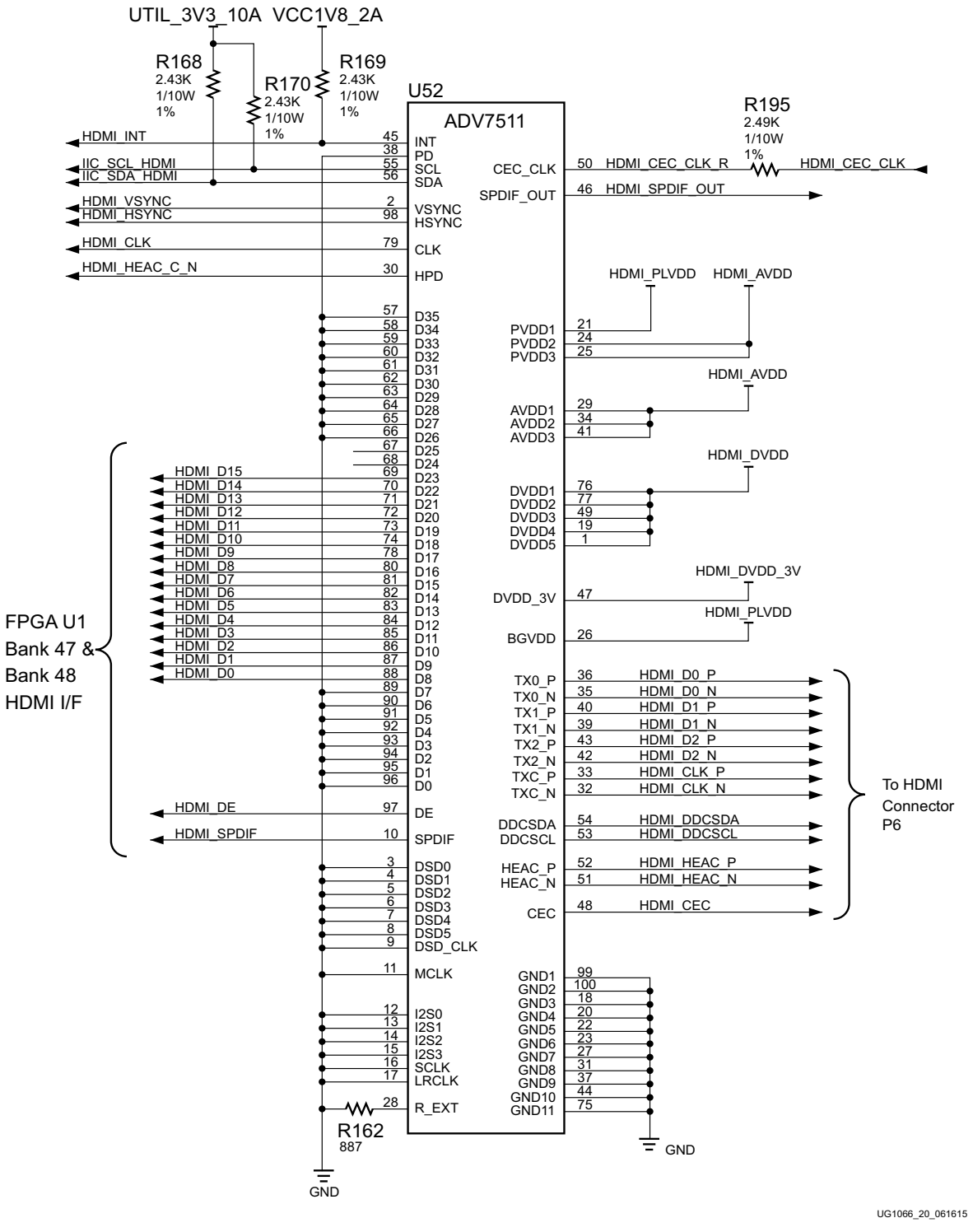


Figure 1-19: **HDMI Codec Circuit**

Table 1-29 lists the HDMI Codec U52 to the XCVU095 device U1 connections. All HDMI nets in this table are series resistor coupled.

Table 1-29: **HDMI Codec U52 to XCVU095 Device U1 Connections**

FPGA (U1) Pin	Schematic Net Name	FPGA (U1) Direction	I/O Standard	ADV7511 U52	
				Pin Number	Name
R36	HDMI_D0	Output	LVCMOS18	88	D8
R34	HDMI_D1	Output	LVCMOS18	87	D9
P34	HDMI_D2	Output	LVCMOS18	86	D10
V30	HDMI_D3	Output	LVCMOS18	85	D11
V33	HDMI_D4	Output	LVCMOS18	84	D12
V34	HDMI_D5	Output	LVCMOS18	83	D13
U35	HDMI_D6	Output	LVCMOS18	82	D14
T36	HDMI_D7	Output	LVCMOS18	81	D15
Y34	HDMI_D8	Output	LVCMOS18	80	D16
W34	HDMI_D9	Output	LVCMOS18	78	D17
V32	HDMI_D10	Output	LVCMOS18	74	D18
U33	HDMI_D11	Output	LVCMOS18	73	D19
AH33	HDMI_D12	Output	LVCMOS18	72	D20
AH30	HDMI_D13	Output	LVCMOS18	71	D21
AM33	HDMI_D14	Output	LVCMOS18	70	D22
AM31	HDMI_D15	Output	LVCMOS18	69	D23
AH34	HDMI_DE	Output	LVCMOS18	97	DE
AJ35	HDMI_SPDIF	Output	LVCMOS18	10	SPDIF
AK33	HDMI_CLK	Output	LVCMOS18	79	CLK
AK30	HDMI_VSYNC	Output	LVCMOS18	2	VSYNC
AK29	HDMI_HSYNC	Output	LVCMOS18	98	HSYNC
AJ33	HDMI_INT	Input	LVCMOS18	45	INT
AJ36	HDMI_SPDIF_OUT	Input	LVCMOS18	46	SPDIF_OUT

For more information about the Analog Devices ADV7511KSTZ-P, see the Analog Devices website [Ref 21]. For additional information about HDMI IP options, see the *DisplayPort LogiCORE IP Product Guide* (PG064) [Ref 22].

I2C Bus, Topology, and Switches

[Figure 1-2, callouts 21, 22]

The VCU108 evaluation board implements a 2-to-1 I2C bus arrangement. A single I2C bus from the FPGA U1 XCVU095 (IIC_MAIN_SCL/SDA_LS) and system controller Zynq-7000 SoC U111 (SYSCTLR_I2C_SCL/SDA) are wired to the same I2C bus using level shifters. FPGA U1 is wired through level shifter U77 and system controller U111 is wired through level shifter U108. The output sides of U77 and U108 are wired in parallel to a common I2C bus (IIC_SDA and _SCL_MAIN). This common I2C bus is then routed to a pair of bus switches, a TI TCA9548 1-to-8 channel I2C bus switch (U28) and a TI PCA9544 1-to-4 channel I2C bus switch (U80). The bus switches can operate at speeds up to 400 kHz. The VCU108 evaluation board I2C bus topology overview is shown in Figure 1-20.

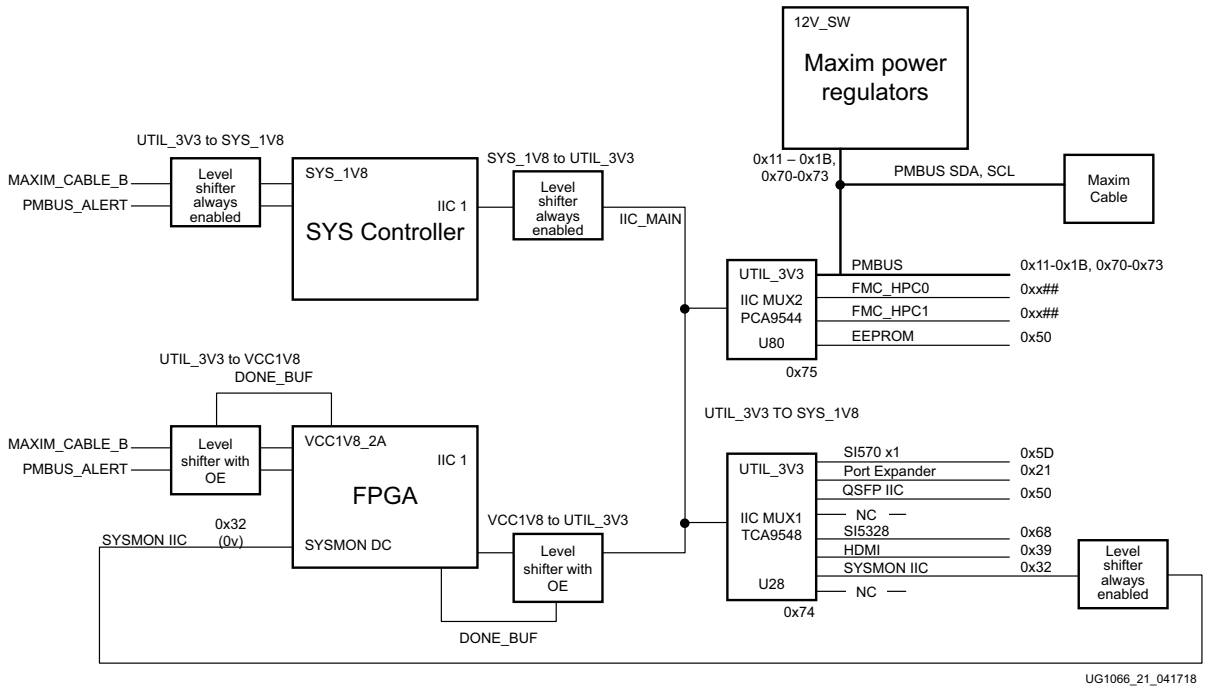


Figure 1-20: **I2C Bus Topology Overview**

IMPORTANT: *The TCA9548 U28 RESET_B pin 3 is connected to FPGA U1 Bank 84 pin AM23 via level shifter U44. The PCA9544 U80 does not have a reset pin. FPGA pin AM23 LVCMOS18 net IIC_MUX_RESET_B_LS must be driven High to enable I2C bus transactions with the devices connected to U28.*

User applications that communicate with devices on one of the downstream I2C buses must first set up a path to the desired bus through the U28 or U80 bus switch at I2C address 0x74 (**0b1110100**) or 0x75 (**0b111101**), respectively. Table 1-30 lists the address for each bus.

Table 1-30: **I2C Bus Addresses**

I2C Devices	I2C Switch Position	I2C Address		Device
		Binary Format	Hex Format	
TCA9548 8-Channel bus switch	N/A	**0b1110100**	**0x74**	U28 TCA9548
SI570 clock	0	**0b1011101**	**0x5D**	U32 SI570
I2C port expander	1	**0b0100001**	**0x21**	U89 TCA6416
QSFP+ module	2	**0b1010000**	**0x50**	U145 28 Gb/s QSFP+
Not used	3	N/A	N/A	N/A
SI5328 clock	4	**0b1101000**	**0x68**	U57 SI5328B
ADV7511 HDMI	5	**0b0111001**	**0x39**	U52 ADV7511
FPGA SYSMON	6	**0b0110010**	**0x32**	U1 BANK 65
Not used	7	N/A	N/A	N/A
PCA9544 4-Channel bus switch	N/A	**0b1110101**	**0x75**	U80 PCA9544
PMBus regulators	0	**0b0010001 - 0b0011011, 0b1110000 - 0b1110011**	**0x11-0x1B, 0x70-0x73**	Various Maxim regulators.(1)
FMC HPC0	2	**0bXXXXXXX**	**0x##**	J22 FMC HPC
FMC HPC1	3	**0bXXXXXXX**	**0x##**	J2 FMC HPC
I2C EEPROM	4	**0b1010000**	**0x50**	U12 M24C08

Notes:

1. MAX15301:U4,U9,U30,U150,U156; MAX20751EKX U164,U165,U166

Information about the TCA9548 and PCA9544 is available on the TI Semiconductor website [Ref 23].

For additional information on the Zynq-7000 SoC device I2C controller, see *Zynq-7000 SoC Overview* (DS190) [Ref 24] and *Zynq-7000 SoC Technical Reference Manual* (UG585) [Ref 25].

Status and User LEDs

Table 1-31 defines VCU108 board status and user LEDs.

Table 1-31: **VCU108 Board Status and User LEDs**

Reference Designator	Description
DS2	INIT
DS3	OR'D POWER GOOD
DS6	GPIO_LED_1
DS7	GPIO_LED_0
DS8	GPIO_LED_2
DS9	GPIO_LED_5
DS10	GPIO_LED_4
DS14	UTIL_3V3_PGOOD
DS15	MGTAVCC_PGOOD
DS16	VCC1V2_PGOOD
DS17	MGTAVTT_PGOOD
DS19	VADJ_1V8_PGOOD
DS21	VCCINT_PGOOD
DS24	VCC1V8_PGOOD
DS25	MGTVCCAUX_PGOOD
DS26	12V ON
DS27	SYS_2V5 ON
DS28	SYS_1V8 ON
DS31	GPIO_LED_7
DS32	GPIO_LED_6
DS33	GPIO_LED_5
DS34	DONE
DS36	DDR4 C1 VTT ON
DS40	SYS_5V0 ON
DS42	SYSCTLR INIT
DS43	SYSCTLR STATUS
DS44	SYSCTLR DONE
DS45	SYSCTLR ERROR
DS46	SYS_1V0 ON
DS47	DDR4 C2 VTT ON
DS48	RLD3 C1 VTT ON
DS49	5V ON

Table 1-31: **VCU108 Board Status and User LEDs *(Cont'd)***

Reference Designator	Description
EPHY P3 GREEN LED	ENET PHY LINK1000
EPHY P3 YELLOW LED	ENET PHY TX

User I/O

[Figure 1-2, callouts 23-26, 40]

The VCU108 board provides these user and general purpose I/O capabilities:

- Eight user LEDs (callout 23)
  - GPIO_LED[7-0]: DS31, DS32, DS33, DS10, DS19, DS8, DS6, DS7
- Five user pushbuttons and CPU reset switch (callout 24)
  - GPIO_SW [NESWC]: SW10, SW9, SW8, SW6, SW7
  - CPU_RESET: SW5 (callout 25)
- 4-position user DIP switch (callout 26)
  - GPIO_DIP_SW[3:0]: SW12

User GPIO LEDs

[Figure 1-2, callout 23]

Figure 1-21 shows the GPIO LED circuit.

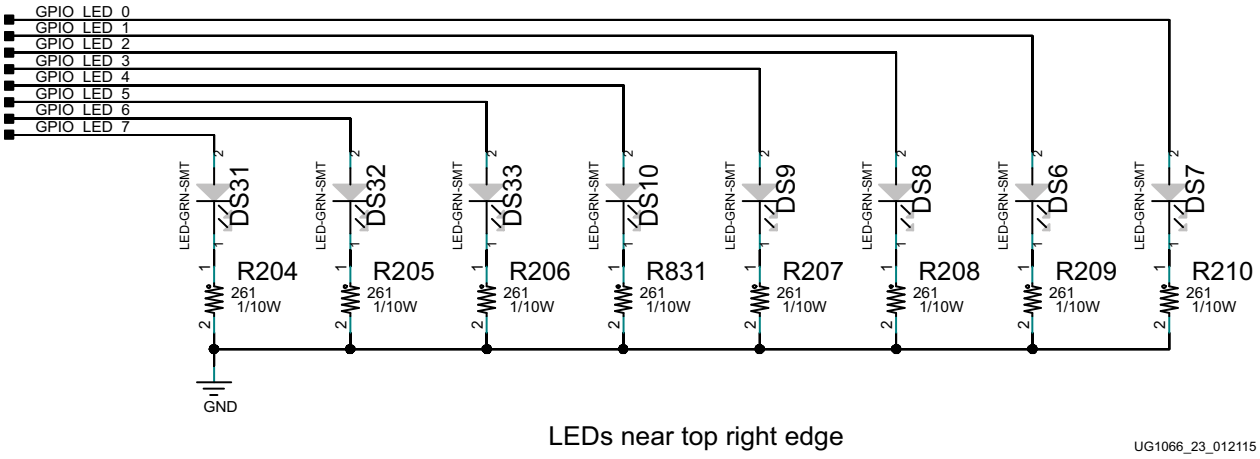


Figure 1-21: **User LEDs**

User Pushbuttons

[Figure 1-2, callout 24]

Figure 1-22 shows the user pushbuttons circuit.

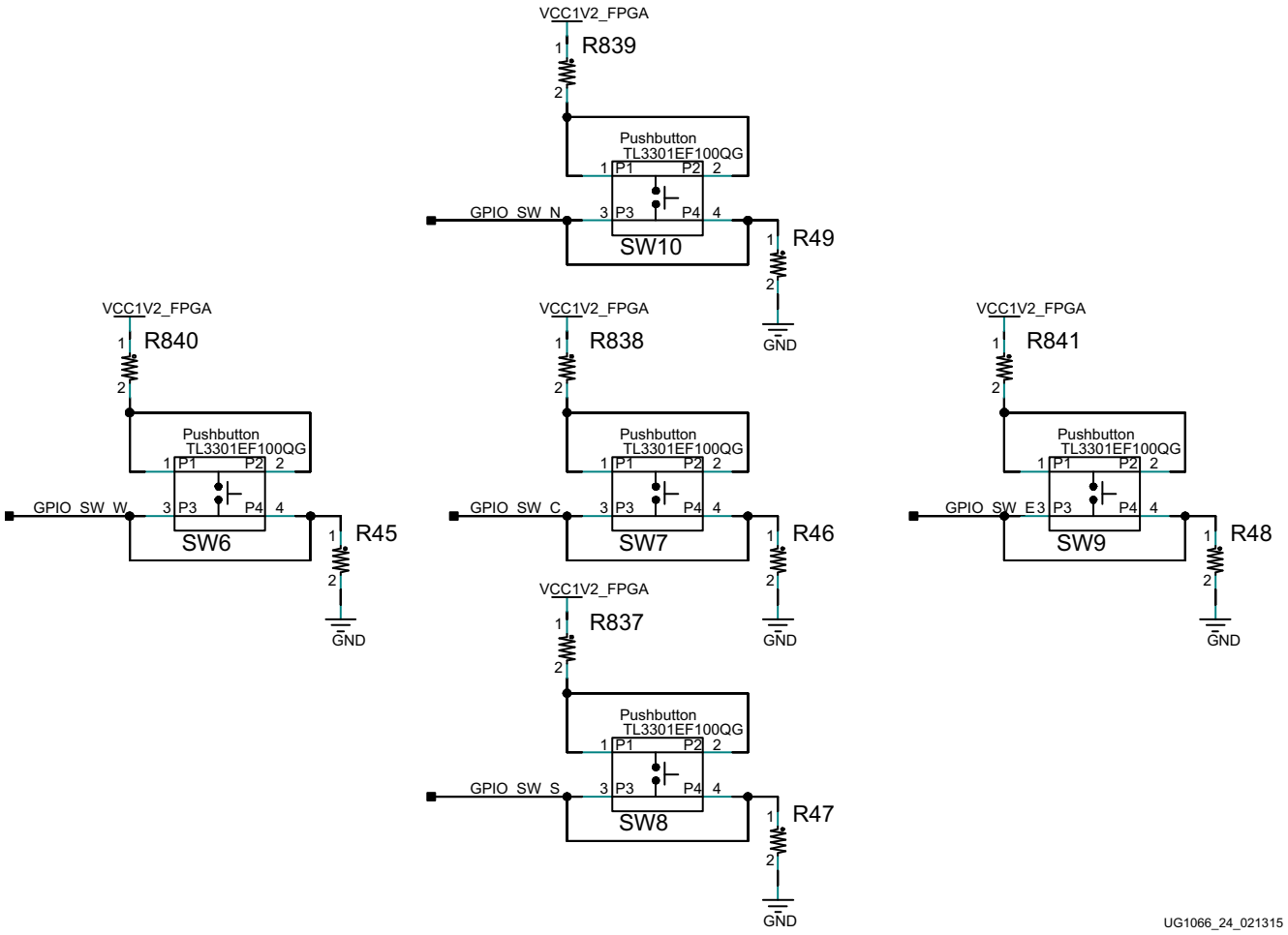


Figure 1-22: **User Pushbuttons**

CPU Reset Pushbutton

[Figure 1-2, callout 25]

Figure 1-23 shows the CPU reset pushbutton circuit.

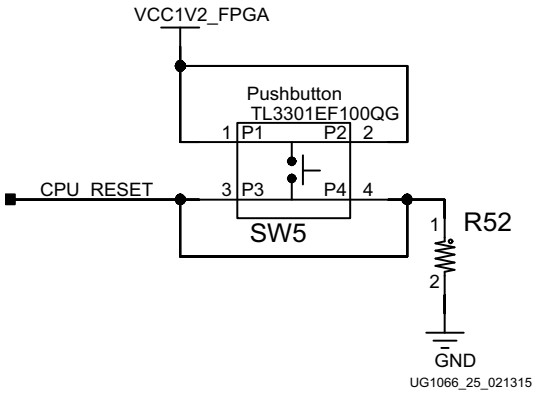


Figure 1-23: **CPU Reset Pushbutton**

GPIO DIP Switch

[Figure 1-2, callout 26]

Figure 1-24 shows the GPIO DIP switch circuit.

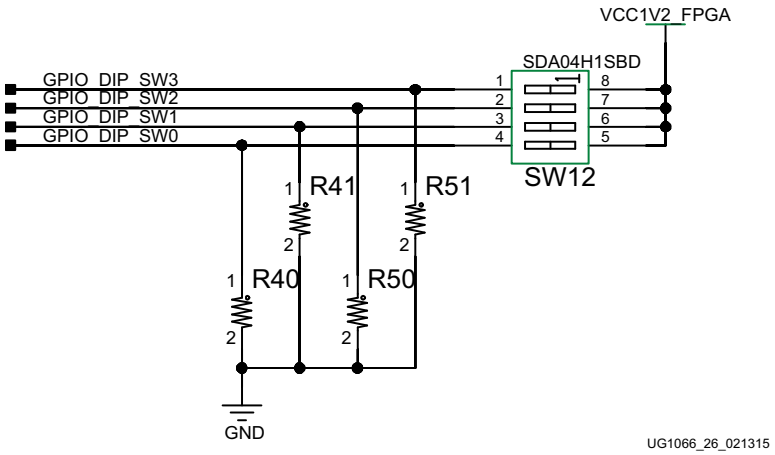


Figure 1-24: **CPU GPIO DIP Switch**

Table 1-32 lists the GPIO connections to FPGA U1.

Table 1-32: **VCU108 GPIO Connections to FPGA U1**

FPGA (U1) Pin		Schematic Net Name	FPGA (U1) Direction	I/O Standard	Device
GPIO LEDs (Active-High)[1]					
BANK 44	AT32	GPIO_LED_0	Output	LVCMOS12	DS7.1
BANK 44	AV34	GPIO_LED_1	Output	LVCMOS12	DS6.1
BANK 44	AY30	GPIO_LED_2	Output	LVCMOS12	DS8.1
BANK 44	BB32	GPIO_LED_3	Output	LVCMOS12	DS9.1
BANK 44	BF32	GPIO_LED_4	Output	LVCMOS12	DS10.1
BANK 46	AV36	GPIO_LED_5	Output	LVCMOS12	DS33.1
BANK 46	AY35	GPIO_LED_6	Output	LVCMOS12	DS32.1
BANK 46	BA37	GPIO_LED_7	Output	LVCMOS12	DS31.1
Directional Pushbuttons (Active-High)					
BANK 501 BANK 49	E34	GPIO_SW_N	Input	LVCMOS12	SW10.3
BANK 501 BANK 69	A10	GPIO_SW_E	Input	LVCMOS12	SW9.3
BANK 501 BANK 70	M22	GPIO_SW_W	Input	LVCMOS12	SW6.3
BANK 501 BANK 69	D9	GPIO_SW_S	Input	LVCMOS12	SW8.3
BANK 501 BANK 49	AW27	GPIO_SW_C	Input	LVCMOS12	SW7.3
4-Pole DIP SW (Active-High)					
BANK 46	BC40	GPIO_DIP_SW0	Input	LVCMOS12	SW12.4
BANK 71	L19	GPIO_DIP_SW1	Input	LVCMOS12	SW12.3
BANK 49	C37	GPIO_DIP_SW2	Input	LVCMOS12	SW12.2
BANK 49	C38	GPIO_DIP_SW3	Input	LVCMOS12	SW12.1

Notes:

1. GPIO_LED signals are level-shifted from 1.2V to 3.3V via U47 and U49.

User Pmod GPIO Headers

[Figure 1-2, callout 29]

The VCU108 evaluation board supports two Pmod GPIO headers J52 and J53. The Pmod nets connected to these headers are accessed using level shifters U41 (PMOD0 J52) and U42 (PMOD1 J53). The level shifters are wired to XCVU095 FPGA U1 banks 66, 67, and 70.

Figure 1-25 shows the GPIO Pmod headers J52 (female right-angle) and J53 (male vertical).

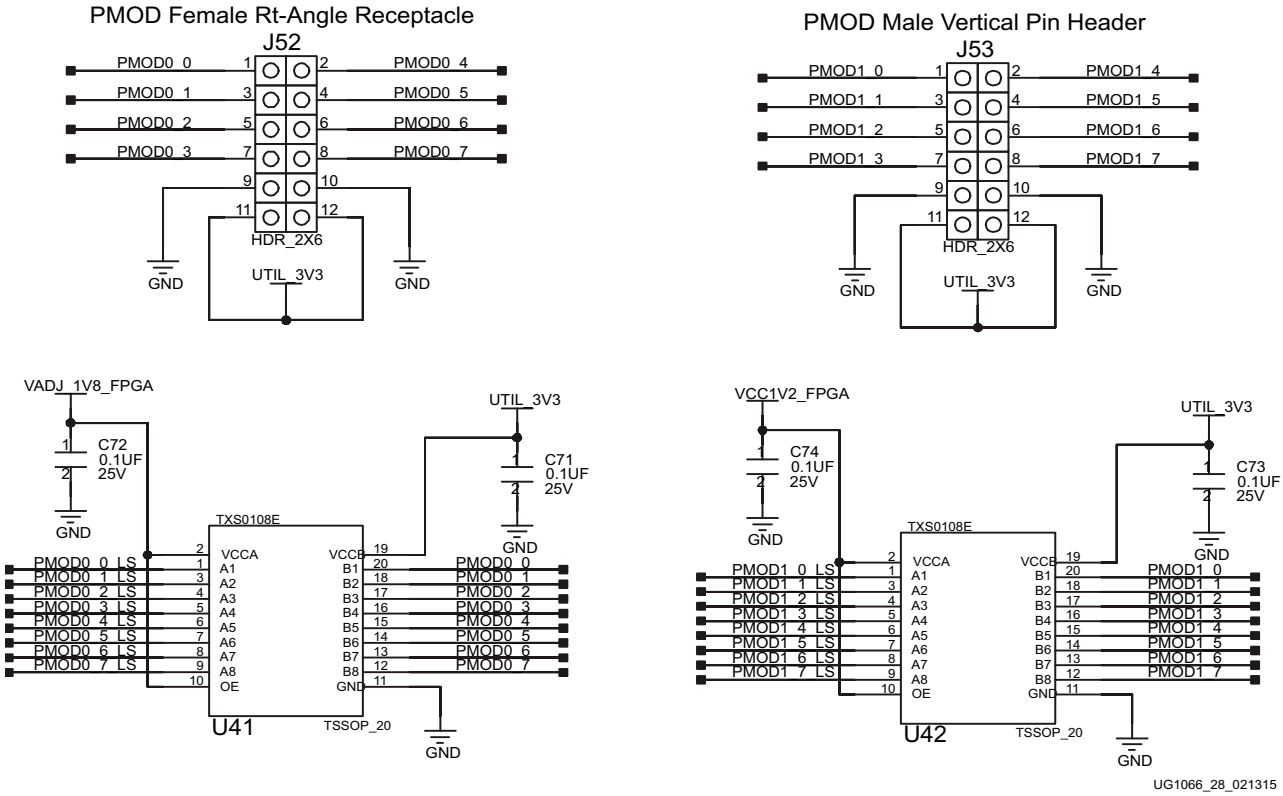


Figure 1-25: **Pmod Connectors J52 and J53 with Level Shifters U42 and U43**

Table 1-33 shows the level shifter U40 and U41 connections to FPGA U1

Table 1-33: **Pmod Connector J52, J53 Connections through Level Shifter U42, U43 to FPGA U1**

FPGA (U1) Pin	Schematic Net Name	I/O Standard	Level Shifter		Schematic Net Name	Pmod Connector Pin
			Side A 1.8V	Side B 3.3V		
BC14	PMOD0_0_LS	LVCMOS18	U41.1	U41.20	PMOD0_0	J52.1
BA10	PMOD0_1_LS	LVCMOS18	U41.3	U41.18	PMOD0_1	J52.3
AW16	PMOD0_2_LS	LVCMOS18	U41.4	U41.17	PMOD0_2	J52.5
BB16	PMOD0_3_LS	LVCMOS18	U41.5	U41.16	PMOD0_3	J52.7
BC13	PMOD0_4_LS	LVCMOS18	U41.6	U41.15	PMOD0_4	J52.2
BF7	PMOD0_5_LS	LVCMOS18	U41.7	U41.14	PMOD0_5	J52.4
AW12	PMOD0_6_LS	LVCMOS18	U41.8	U41.13	PMOD0_6	J52.6
BC16	PMOD0_7_LS	LVCMOS18	U41.9	U41.12	PMOD0_7	J52.8
			Side A 1.2V	**Side B 3.3V**		
P22	PMOD1_0_LS	LVCMOS12	U42.1	U42.20	PMOD1_0	J53.1
N22	PMOD1_1_LS	LVCMOS12	U42.3	U42.18	PMOD1_1	J53.3
J20	PMOD1_2_LS	LVCMOS12	U42.4	U42.17	PMOD1_2	J53.5
K24	PMOD1_3_LS	LVCMOS12	U42.5	U42.16	PMOD1_3	J53.7
J24	PMOD1_4_LS	LVCMOS12	U42.6	U42.15	PMOD1_4	J53.2
T23	PMOD1_5_LS	LVCMOS12	U42.7	U42.14	PMOD1_5	J53.4
R23	PMOD1_6_LS	LVCMOS12	U42.8	U42.13	PMOD1_6	J53.6
R22	PMOD1_7_LS	LVCMOS12	U42.9	U42.12	PMOD1_7	J53.8

For more information about Pmod connector compatible Pmod modules, see the Digilent website [Ref 8].

Switches

[Figure 1-2, callouts 27, 30]

The VCU108 evaluation board includes a power on/off slide switch and a configuration pushbutton switch:

- Power on/off slide switch SW1 (callout 30)
- FPGA Program_B SW4, active-Low (callout 27)

Power On/Off Slide Switch SW1

[Figure 1-2, callout 30]

The VCU108 board power switch is SW1. Sliding the switch actuator from the off to on position applies 12VDC power from the 6-pin mini-fit power input connector J15. Green LED DS26 illuminates when the VCU108 board power is on. See VCU108 Board Power System for details on the onboard power system.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J15 on the VCU108 evaluation board. The ATX 6-pin connector has a different pinout than J15. Connecting an ATX 6-pin connector into J15 damages the VCU108 evaluation board and voids the board warranty.*

The VCU108 evaluation kit provides the adapter cable shown in Figure 1-26 for powering the VCU108 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to the Sourcegate Technologies part number AZCBL-WH-1109-RA4. See [Ref 26] for ordering information.

Figure 1-26: **ATX Power Supply Adapter Cable**

Figure 1-27 shows the power connector J15, power switch SW1, and indicator LED DS26.

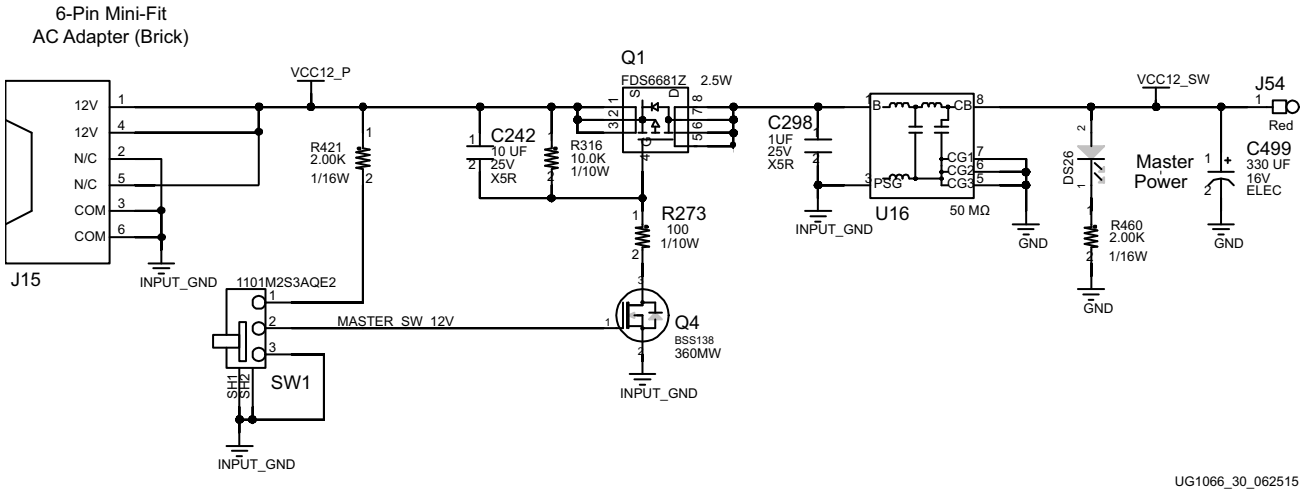


Figure 1-27: **Power On/Off Switch SW1**

Program_B Pushbutton Switch

[Figure 1-2, callout 27]

Switch SW4 grounds the XCVU095 FPGA U1 PROGRAM_B pin when pressed. This action clears the FPGA configuration. The FPGA_PROG_B signal is connected to XCVU095 FPGA U1 pin AH11. See *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2] for further configuration details.

Figure 1-28 shows SW4.

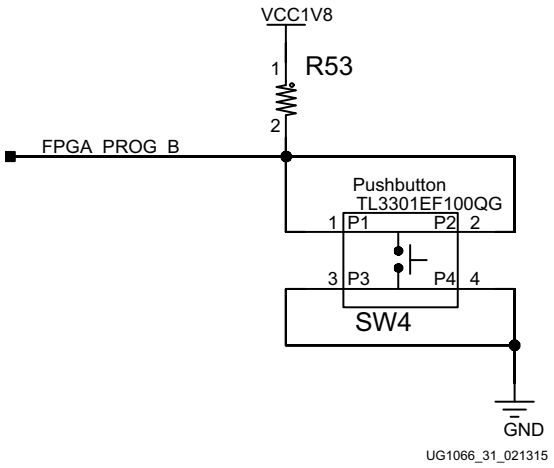


Figure 1-28: **Program_B Pushbutton Switch SW4**

FPGA Mezzanine Card Interface

[Figure 1-2, callouts 33, 34]

The VCU108 evaluation board supports the VITA 57.1 FPGA mezzanine card (FMC) specification by providing subset implementations of high pin count connectors at J22 (HPC0) and J2 (HPC1). HPC connectors use a 10 x 40 form factor, populated with 400 pins. The connectors are keyed so that a mezzanine card, when installed in either of these FMC connectors on the VCU108 evaluation board, faces away from the board.

Connector Type

- Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector. More information about SEAF series connectors is available at the Samtec website [Ref 27]. More information about the VITA 57.1 FMC specification is available at the VITA FMC Marketing Alliance website [Ref 28].
- The 400-pin HPC connector defined by the FMC specification (see Appendix B, VITA 57.1 FMC Connector Pinouts) provides connectivity for up to:
  - 160 single-ended or 80 differential user-defined signals

- 10 transceiver differential pairs
- 2 transceiver differential clocks
- 4 differential clocks
- 159 ground and 15 power connections

FMC HPC0 Connector J22

[Figure 1-2, callout 33]

The HPC connector at J22 implements a subset of the full FMC HPC connectivity:

- 58 differential user-defined pairs (34 LA pairs: LA[00:33]; 24 HA pairs: HA[00:23])
- 10 GTH transceiver differential pairs
- Two GTH transceiver clocks
- Two differential clocks
- 159 ground and 15 power connections

The VCU108 board FMC VADJ voltage VADJ_1V8_FPGA for the J22 and J2 FMC connectors is determined by the MAX15301 U30 voltage regulator described in the VCU108 Board Power System section. The HPC0 J22 connections to FPGA U1 are shown in Table 1-34.

Table 1-34: **J22 VITA 57.1 FMC HPC0 Connections**

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
A/B Connections to FPGA U1							
A2	FMC_HPC0_DP1_M2C_P		H2	B1	NC	NA	NA
A3	FMC_HPC0_DP1_M2C_N		H1	B4	FMC_HPC0_DP9_M2C_P		W4
A6	FMC_HPC0_DP2_M2C_P		F2	B5	FMC_HPC0_DP9_M2C_N		W3
A7	FMC_HPC0_DP2_M2C_N		F1	B8	FMC_HPC0_DP8_M2C_P		Y2
A10	FMC_HPC0_DP3_M2C_P		D2	B9	FMC_HPC0_DP8_M2C_N		Y1
A11	FMC_HPC0_DP3_M2C_N		D1	B12	FMC_HPC0_DP7_M2C_P		M2
A14	FMC_HPC0_DP4_M2C_P		T2	B13	FMC_HPC0_DP7_M2C_N		M1
A15	FMC_HPC0_DP4_M2C_N		T1	B16	FMC_HPC0_DP6_M2C_P		P2
A18	FMC_HPC0_DP5_M2C_P		R4	B17	FMC_HPC0_DP6_M2C_N		P1
A19	FMC_HPC0_DP5_M2C_N		R3	B20	FMC_HPC0_GBTCLK1_M2C_P	(1)	N9
A22	FMC_HPC0_DP1_C2M_P		F7	B21	FMC_HPC0_GBTCLK1_M2C_N	(1)	N8
A23	FMC_HPC0_DP1_C2M_N		F6	B24	FMC_HPC0_DP9_C2M_P		T7
A26	FMC_HPC0_DP2_C2M_P		E5	B25	FMC_HPC0_DP9_C2M_N		T6
A27	FMC_HPC0_DP2_C2M_N		E4	B28	FMC_HPC0_DP8_C2M_P		V7
A30	FMC_HPC0_DP3_C2M_P		C5	B29	FMC_HPC0_DP8_C2M_N		V6

Table 1-34: **J22 VITA 57.1 FMC HPC0 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
A31	FMC_HPC0_DP3_C2M_N		C4	B32	FMC_HPC0_DP7_C2M_P		H7
A34	FMC_HPC0_DP4_C2M_P		L5	B33	FMC_HPC0_DP7_C2M_N		H6
A35	FMC_HPC0_DP4_C2M_N		L4	B36	FMC_HPC0_DP6_C2M_P		J5
A38	FMC_HPC0_DP5_C2M_P		K7	B37	FMC_HPC0_DP6_C2M_N		J4
A39	FMC_HPC0_DP5_C2M_N		K6	B40	NC	NA	NA
C/D Connections to FPGA U1							
C2	FMC_HPC0_DP0_C2M_P		G5	D1	VADJ_1V8_PGOOD(2)		U44.20
C3	FMC_HPC0_DP0_C2M_N		G4	D4	FMC_HPC0_GBTCLK0_M2C_P	(1)	R9
C6	FMC_HPC0_DP0_M2C_P		K2	D5	FMC_HPC0_GBTCLK0_M2C_N	(1)	R8
C7	FMC_HPC0_DP0_M2C_N		K1	D8	FMC_HPC0_LA01_CC_P	LVDS	BC10
C10	FMC_HPC0_LA06_P	LVDS	BE10	D9	FMC_HPC0_LA01_CC_N	LVDS	BD10
C11	FMC_HPC0_LA06_N	LVDS	BE9	D11	FMC_HPC0_LA05_P	LVDS	BF12
C14	FMC_HPC0_LA10_P	LVDS	BE14	D12	FMC_HPC0_LA05_N	LVDS	BF11
C15	FMC_HPC0_LA10_N	LVDS	BF14	D14	FMC_HPC0_LA09_P	LVDS	BD13
C18	FMC_HPC0_LA14_P	LVDS	BB13	D15	FMC_HPC0_LA09_N	LVDS	BE13
C19	FMC_HPC0_LA14_N	LVDS	BB12	D17	FMC_HPC0_LA13_P	LVDS	BA14
C22	FMC_HPC0_LA18_CC_P	LVDS	AP13	D18	FMC_HPC0_LA13_N	LVDS	BB14
C23	FMC_HPC0_LA18_CC_N	LVDS	AR13	D20	FMC_HPC0_LA17_CC_P	LVDS	AV14
C26	FMC_HPC0_LA27_P	LVDS	AN14	D21	FMC_HPC0_LA17_CC_N	LVDS	AV13
C27	FMC_HPC0_LA27_N	LVDS	AN13	D23	FMC_HPC0_LA23_P	LVDS	AT16
C30	FMC_HPC0_IIC_SCL(6)		U80.9	D24	FMC_HPC0_LA23_N	LVDS	AT15
C31	FMC_HPC0_IIC_SDA(6)		U80.8	D26	FMC_HPC0_LA26_P	LVDS	AL14
C34	GA0 = 0 = GND			D27	FMC_HPC0_LA26_N	LVDS	AM14
C35	VCC12_SW			D29	FMC_HPC0_TCK_BUF(3)		U19.17
C37	VCC12_SW			D30	FPGA_TDO_FMC_TDI_BUF(4)		U19.21, U26.1
C39	UTIL_3V3			D31	FMC_HPC0_TDO_HPC1_TDI(3)(4)		U26.2, U132.1, J2.D30
				D32	UTIL_3V3		
				D33	FMC_HPC0_TMS_BUF(3)		U19.20
				D34	NC		
				D35	GA1 = 0 = GND		
				D36	UTIL_3V3		
				D38	UTIL_3V3		
				D40	UTIL_3V3		

Table 1-34: **J22 VITA 57.1 FMC HPC0 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
E/F Connections to FPGA U1							
E2	FMC_HPC0_HA01_CC_P	LVDS	T14	F1	FMC_HPC0_PG_M2C(7)	LVCMOS18	U44.18
E3	FMC_HPC0_HA01_CC_N	LVDS	R13	F4	FMC_HPC0_HA00_CC_P	LVDS	N14
E6	FMC_HPC0_HA05_P	LVDS	AA12	F5	FMC_HPC0_HA00_CC_N	LVDS	N13
E7	FMC_HPC0_HA05_N	LVDS	Y12	F7	FMC_HPC0_HA04_P	LVDS	AA13
E9	FMC_HPC0_HA09_P	LVDS	AA14	F8	FMC_HPC0_HA04_N	LVDS	Y13
E10	FMC_HPC0_HA09_N	LVDS	Y14	F10	FMC_HPC0_HA08_P	LVDS	W12
E12	FMC_HPC0_HA13_P	LVDS	W14	F11	FMC_HPC0_HA08_N	LVDS	V12
E13	FMC_HPC0_HA13_N	LVDS	V14	F13	FMC_HPC0_HA12_P	LVDS	V15
E15	FMC_HPC0_HA16_P	LVDS	V16	F14	FMC_HPC0_HA12_N	LVDS	U15
E16	FMC_HPC0_HA16_N	LVDS	U16	F16	FMC_HPC0_HA15_P	LVDS	V13
E18	FMC_HPC0_HA20_P	LVDS	R11	F17	FMC_HPC0_HA15_N	LVDS	U12
E19	FMC_HPC0_HA20_N	LVDS	P11	F19	FMC_HPC0_HA19_P	LVDS	R14
E21	NC	NA	NA	F20	FMC_HPC0_HA19_N	LVDS	P14
E22	NC	NA	NA	F22	NC	NA	NA
E24	NC	NA	NA	F23	NC	NA	NA
E25	NC	NA	NA	F25	NC	NA	NA
E27	NC	NA	NA	F26	NC	NA	NA
E28	NC	NA	NA	F28	NC	NA	NA
E30	NC	NA	NA	F29	NC	NA	NA
E31	NC	NA	NA	F31	NC	NA	NA
E33	NC	NA	NA	F32	NC	NA	NA
E34	NC	NA	NA	F34	NC	NA	NA
E36	NC	NA	NA	F35	NC	NA	NA
E37	NC	NA	NA	F37	NC	NA	NA
E39	VADJ _1V8_FPGA			F38	NC	NA	NA
				F40	VADJ _1V8_FPGA		
G/H Connections to FPGA U1							
G2	FMC_HPC0_CLK1_M2C_P	LVDS	AU14	H1	FMC_HPC0_VREF_A_M2C		U1.AL16
G3	FMC_HPC0_CLK1_M2C_N	LVDS	AU13	H2	FMC_HPC0_PRSNT_M2C_B(5)	LVCMOS18	U26.4, U44.18, U109.18, AL19
G6	FMC_HPC0_LA00_CC_P	LVDS	AY9	H4	FMC_HPC0_CLK0_M2C_P	LVCMOS18	BB9
G7	FMC_HPC0_LA00_CC_N	LVDS	BA9	H5	FMC_HPC0_CLK0_M2C_N	LVCMOS18	BB8
G9	FMC_HPC0_LA03_P	LVDS	BD8	H7	FMC_HPC0_LA02_P	LVDS	BA7
G10	FMC_HPC0_LA03_N	LVDS	BD7	H8	FMC_HPC0_LA02_N	LVDS	BB7
G12	FMC_HPC0_LA08_P	LVDS	BF10	H10	FMC_HPC0_LA04_P	LVDS	BE8

Table 1-34: **J22 VITA 57.1 FMC HPC0 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
G13	FMC_HPC0_LA08_N	LVDS	BF9	H11	FMC_HPC0_LA04_N	LVDS	BE7
G15	FMC_HPC0_LA12_P	LVDS	BE15	H13	FMC_HPC0_LA07_P	LVDS	BD12
G16	FMC_HPC0_LA12_N	LVDS	BF15	H14	FMC_HPC0_LA07_N	LVDS	BE12
G18	FMC_HPC0_LA16_P	LVDS	AY8	H16	FMC_HPC0_LA11_P	LVDS	BC11
G19	FMC_HPC0_LA16_N	LVDS	AY7	H17	FMC_HPC0_LA11_N	LVDS	BD11
G21	FMC_HPC0_LA20_P	LVDS	AY15	H19	FMC_HPC0_LA15_P	LVDS	AV9
G22	FMC_HPC0_LA20_N	LVDS	AY14	H20	FMC_HPC0_LA15_N	LVDS	AV8
G24	FMC_HPC0_LA22_P	LVDS	AN15	H22	FMC_HPC0_LA19_P	LVDS	AV15
G25	FMC_HPC0_LA22_N	LVDS	AP15	H23	FMC_HPC0_LA19_N	LVDS	AW15
G27	FMC_HPC0_LA25_P	LVDS	AM13	H25	FMC_HPC0_LA21_P	LVDS	AN16
G28	FMC_HPC0_LA25_N	LVDS	AM12	H26	FMC_HPC0_LA21_N	LVDS	AP16
G30	FMC_HPC0_LA29_P	LVDS	AK14	H28	FMC_HPC0_LA24_P	LVDS	AK15
G31	FMC_HPC0_LA29_N	LVDS	AK13	H29	FMC_HPC0_LA24_N	LVDS	AL15
G33	FMC_HPC0_LA31_P	LVDS	AP12	H31	FMC_HPC0_LA28_P	LVDS	AJ13
G34	FMC_HPC0_LA31_N	LVDS	AR12	H32	FMC_HPC0_LA28_N	LVDS	AJ12
G36	FMC_HPC0_LA33_P	LVDS	AU16	H34	FMC_HPC0_LA30_P	LVDS	AK12
G37	FMC_HPC0_LA33_N	LVDS	AV16	H35	FMC_HPC0_LA30_N	LVDS	AL12
G39	VADJ _1V8_FPGA			H37	FMC_HPC0_LA32_P	LVDS	AU11
				H38	FMC_HPC0_LA32_N	LVDS	AV11
				H40	VADJ _1V8_FPGA		
J/K Connections to FPGA U1							
J2	NC	NA	NA	K1	NC	NA	NA
J3	NC	NA	NA	K4	NC	NA	NA
J6	FMC_HPC0_HA03_P	LVDS	K11	K5	NC	NA	NA
J7	FMC_HPC0_HA03_N	LVDS	J11	K7	FMC_HPC0_HA02_P	LVDS	T16
J9	FMC_HPC0_HA07_P	LVDS	R12	K8	FMC_HPC0_HA02_N	LVDS	T15
J10	FMC_HPC0_HA07_N	LVDS	P12	K10	FMC_HPC0_HA06_P	LVDS	P15
J12	FMC_HPC0_HA11_P	LVDS	M11	K11	FMC_HPC0_HA06_N	LVDS	N15
J13	FMC_HPC0_HA11_N	LVDS	L11	K13	FMC_HPC0_HA10_P	LVDS	K12
J15	FMC_HPC0_HA14_P	LVDS	K14	K14	FMC_HPC0_HA10_N	LVDS	J12
J16	FMC_HPC0_HA14_N	LVDS	K13	K16	FMC_HPC0_HA17_CC_P	LVDS	U13
J18	FMC_HPC0_HA18_P	LVDS	L14	K17	FMC_HPC0_HA17_CC_N	LVDS	T13

Table 1-34: **J22 VITA 57.1 FMC HPC0 Connections *(Cont'd)***

J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J22 FMC HPC0 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J19	FMC_HPC0_HA18_N	LVDS	L13	K19	FMC_HPC0_HA21_P	LVDS	M13
J21	FMC_HPC0_HA22_P	LVDS	M15	K20	FMC_HPC0_HA21_N	LVDS	M12
J22	FMC_HPC0_HA22_N	LVDS	L15	K22	FMC_HPC0_HA23_P	LVDS	U11
J24	NC	NA	NA	K23	FMC_HPC0_HA23_N	LVDS	T11
J25	NC	NA	NA	K25	NC	NA	NA
J27	NC	NA	NA	K26	NC	NA	NA
J28	NC	NA	NA	K28	NC	NA	NA
J30	NC	NA	NA	K29	NC	NA	NA
J31	NC	NA	NA	K31	NC	NA	NA
J33	NC	NA	NA	K32	NC	NA	NA
J34	NC	NA	NA	K34	NC	NA	NA
J36	NC	NA	NA	K35	NC	NA	NA
J37	NC	NA	NA	K37	NC	NA	NA
J39	NC	NA	NA	K38	NC	NA	NA
				K40	NC	NA	NA

Notes:
1. Series capacitor coupled to the XCVU095 U1 pin.
2. U30 MAX15301 VADJ_1V8_FPGA voltage regulator power good output signal.
3. FPGA U1 JTAG TCK, TMS, TDO pins AE13, AF15, AD13 buffered by U19 SN74AVC8T245.
4. J22 HPC0 TDO-TDI connections to U26 HPC FMC JTAG bypass switch (N.C. normally closes/bypassing J22 until an FMC card is plugged into J22).
5. FMC_HPC0_PRSNT_M2C_B is the HPC0 FMC JTAG bypass switch U26.4 OE control signal and is also connected to the FPGA U1 pin AL19 via level shifter U44.
6. Connected to the FPGA U1 LS pins AP21/AN21 IIC_MAIN_SDA/SCL via IIC MUX U80 and level shifter U77.
7. HPC0 FMC signal FMC_HPC0_PG_M2C is connected to the FPGA U1 pin AP22 via level shifter U44.

FMC HPC1 Connector J2

[Figure 1-2, callout 34]

The HPC connector at J2 implements a subset of the full FMC HPC connectivity:

- 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- Ten GTH transceiver differential pairs
- Two GTH transceiver clocks
- Two differential clocks
- 159 ground and 15 power connections

The HPC1 J2 connections to FPGA U1 are documented in Table 1-35.

Table 1-35: **J2 VITA 57.1 FMC HPC1 Connections**

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
A/B Connections to FPGA U1							
A2	FMC_HPC1_DP1_M2C_P		AG4	B1	NC	NA	NA
A3	FMC_HPC1_DP1_M2C_N		AG3	B4	FMC_HPC1_DP9_M2C_P		W4
A6	FMC_HPC1_DP2_M2C_P		AF2	B5	FMC_HPC1_DP9_M2C_N		W3
A7	FMC_HPC1_DP2_M2C_N		AF1	B8	FMC_HPC1_DP8_M2C_P		Y2
A10	FMC_HPC1_DP3_M2C_P		AE4	B9	FMC_HPC1_DP8_M2C_N		Y1
A11	FMC_HPC1_DP3_M2C_N		AE3	B12	FMC_HPC1_DP7_M2C_P		AA4
A14	FMC_HPC1_DP4_M2C_P		AD2	B13	FMC_HPC1_DP7_M2C_N		AA3
A15	FMC_HPC1_DP4_M2C_N		AD1	B16	FMC_HPC1_DP6_M2C_P		AB2
A18	FMC_HPC1_DP5_M2C_P		AC4	B17	FMC_HPC1_DP6_M2C_N		AB1
A19	FMC_HPC1_DP5_M2C_N		AC3	B20	FMC_HPC1_GBTCLK1_M2C_P	(1)	AA9
A22	FMC_HPC1_DP1_C2M_P		AM7	B21	FMC_HPC1_GBTCLK1_M2C_N	(1)	AA8
A23	FMC_HPC1_DP1_C2M_N		AM6	B24	FMC_HPC1_DP9_C2M_P		T7
A26	FMC_HPC1_DP2_C2M_P		AK7	B25	FMC_HPC1_DP9_C2M_N		T6
A27	FMC_HPC1_DP2_C2M_N		AK6	B28	FMC_HPC1_DP8_C2M_P		V7
A30	FMC_HPC1_DP3_C2M_P		AH7	B29	FMC_HPC1_DP8_C2M_N		V6
A31	FMC_HPC1_DP3_C2M_N		AH6	B32	FMC_HPC1_DP7_C2M_P		Y7
A34	FMC_HPC1_DP4_C2M_P		AF7	B33	FMC_HPC1_DP7_C2M_N		Y6
A35	FMC_HPC1_DP4_C2M_N		AF6	B36	FMC_HPC1_DP6_C2M_P		AB7
A38	FMC_HPC1_DP5_C2M_P		AD7	B37	FMC_HPC1_DP6_C2M_N		AB6
A39	FMC_HPC1_DP5_C2M_N		AD6	B40	NC	NA	NA
C/D Connections to FPGA U1							
C2	FMC_HPC1_DP0_C2M_P		AN5	D1	VADJ_1V8_PGOOD(2)		U44.20
C3	FMC_HPC1_DP0_C2M_N		AN4	D4	FMC_HPC1_GBTCLK0_M2C_P	(1)	
C6	FMC_HPC1_DP0_M2C_P		AH2	D5	FMC_HPC1_GBTCLK0_M2C_N	(1)	
C7	FMC_HPC1_DP0_M2C_N		AH1	D8	FMC_HPC1_LA01_CC_P	LVDS	P35
C10	FMC_HPC1_LA06_P	LVDS	P37	D9	FMC_HPC1_LA01_CC_N	LVDS	P36
C11	FMC_HPC1_LA06_N	LVDS	N37	D11	FMC_HPC1_LA05_P	LVDS	N38
C14	FMC_HPC1_LA10_P	LVDS	N32	D12	FMC_HPC1_LA05_N	LVDS	M38
C15	FMC_HPC1_LA10_N	LVDS	M32	D14	FMC_HPC1_LA09_P	LVDS	M36
C18	FMC_HPC1_LA14_P	LVDS	L33	D15	FMC_HPC1_LA09_N	LVDS	L36
C19	FMC_HPC1_LA14_N	LVDS	K33	D17	FMC_HPC1_LA13_P	LVDS	T30
C22	FMC_HPC1_LA18_CC_P	LVDS	AL32	D18	FMC_HPC1_LA13_N	LVDS	T31
C23	FMC_HPC1_LA18_CC_N	LVDS	AM32	D20	FMC_HPC1_LA17_CC_P	LVDS	AJ32
C26	FMC_HPC1_LA27_P	LVDS	AP35	D21	FMC_HPC1_LA17_CC_N	LVDS	AK32

Table 1-35: **J2 VITA 57.1 FMC HPC1 Connections *(Cont'd)***

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
C27	FMC_HPC1_LA27_N	LVDS	AR35	D23	FMC_HPC1_LA23_P	LVDS	AN33
C30	FMC_HPC1_IIC_SCL(6)		U80.13	D24	FMC_HPC1_LA23_N	LVDS	AP33
C31	FMC_HPC1_IIC_SDA(6)		U80.12	D26	FMC_HPC1_LA26_P	LVDS	AL29
C34	GA0 = 0 = GND			D27	FMC_HPC1_LA26_N	LVDS	AM29
C35	VCC12_SW			D29	FMC_HPC1_TCK_BUF(3)		U19.16
C37	VCC12_SW			D30	FMC_HPC0_TDO_HPC1_TDI(4)		U132
C39	UTIL_3V3			D31	FMC_HPC1_TDO(3)(4)		U132
				D32	UTIL_3V3		
				D33	FMC_HPC1_TMS_BUF(3)		U19.19
				D34	NC		
				D35	GA1 = 0 = GND		
				D36	UTIL_3V3		
				D38	UTIL_3V3		
				D40	UTIL_3V3		
E/F Connections to FPGA U1							
E2	NC	NA	NA	F1	FMC_HPC1_PG_M2C(7)	LVCMOS18	AU24
E3	NC	NA	NA	F4	NC	NA	NA
E6	NC	NA	NA	F5	NC	NA	NA
E7	NC	NA	NA	F7	NC	NA	NA
E9	NC	NA	NA	F8	NC	NA	NA
E10	NC	NA	NA	F10	NC	NA	NA
E12	NC	NA	NA	F11	NC	NA	NA
E13	NC	NA	NA	F13	NC	NA	NA
E15	NC	NA	NA	F14	NC	NA	NA
E16	NC	NA	NA	F16	NC	NA	NA
E18	NC	NA	NA	F17	NC	NA	NA
E19	NC	NA	NA	F19	NC	NA	NA
E21	NC	NA	NA	F20	NC	NA	NA
E22	NC	NA	NA	F22	NC	NA	NA
E24	NC	NA	NA	F23	NC	NA	NA
E25	NC	NA	NA	F25	NC	NA	NA
E27	NC	NA	NA	F26	NC	NA	NA
E28	NC	NA	NA	F28	NC	NA	NA
E30	NC	NA	NA	F29	NC	NA	NA
E31	NC	NA	NA	F31	NC	NA	NA
E33	NC	NA	NA	F32	NC	NA	NA
E34	NC	NA	NA	F34	NC	NA	NA

Table 1-35: **J2 VITA 57.1 FMC HPC1 Connections *(Cont'd)***

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
E36	NC	NA	NA	F35	NC	NA	NA
E37	NC	NA	NA	F37	NC	NA	NA
E39	VADJ_1V8_FPGA			F38	NC	NA	NA
				F40	VADJ_1V8_FPGA		
G/H Connections to FPGA U1							
G2	FMC_HPC1_CLK1_M2C_P		AK34	H1	FMC_HPC1_VREF_A_M2C	LVCMOS18	(2)
G3	FMC_HPC1_CLK1_M2C_N		AL34	H2	FMC_HPC1_PRSNT_M2C_B(5)	LVCMOS18	U44.16,U109.1, U132.4, BD23
G6	FMC_HPC1_LA00_CC_P	LVDS	T33	H4	FMC_HPC1_CLK0_M2C_P	LVDS	R32
G7	FMC_HPC1_LA00_CC_N	LVDS	R33	H5	FMC_HPC1_CLK0_M2C_N	LVDS	P32
G9	FMC_HPC1_LA03_P	LVDS	N34	H7	FMC_HPC1_LA02_P	LVDS	N33
G10	FMC_HPC1_LA03_N	LVDS	N35	H8	FMC_HPC1_LA02_N	LVDS	M33
G12	FMC_HPC1_LA08_P	LVDS	M35	H10	FMC_HPC1_LA04_P	LVDS	M37
G13	FMC_HPC1_LA08_N	LVDS	L35	H11	FMC_HPC1_LA04_N	LVDS	L38
G15	FMC_HPC1_LA12_P	LVDS	R31	H13	FMC_HPC1_LA07_P	LVDS	L34
G16	FMC_HPC1_LA12_N	LVDS	P31	H14	FMC_HPC1_LA07_N	LVDS	K34
G18	FMC_HPC1_LA16_P	LVDS	U31	H16	FMC_HPC1_LA11_P	LVDS	Y31
G19	FMC_HPC1_LA16_N	LVDS	U32	H17	FMC_HPC1_LA11_N	LVDS	W31
G21	FMC_HPC1_LA20_P	LVDS	AR37	H19	FMC_HPC1_LA15_P	LVDS	T34
G22	FMC_HPC1_LA20_N	LVDS	AT37	H20	FMC_HPC1_LA15_N	LVDS	T35
G24	FMC_HPC1_LA22_P	LVDS	AL30	H22	FMC_HPC1_LA19_P	LVDS	AT39
G25	FMC_HPC1_LA22_N	LVDS	AL31	H23	FMC_HPC1_LA19_N	LVDS	AT40
G27	FMC_HPC1_LA25_P	LVDS	AP36	H25	FMC_HPC1_LA21_P	LVDS	AT35
G28	FMC_HPC1_LA25_N	LVDS	AP37	H26	FMC_HPC1_LA21_N	LVDS	AT36
G30	FMC_HPC1_LA29_P	LVDS	AP38	H28	FMC_HPC1_LA24_P	LVDS	AM36
G31	FMC_HPC1_LA29_N	LVDS	AR38	H29	FMC_HPC1_LA24_N	LVDS	AN36
G33	FMC_HPC1_LA31_P	LVDS	AN34	H31	FMC_HPC1_LA28_P	LVDS	AL35
G34	FMC_HPC1_LA31_N	LVDS	AN35	H32	FMC_HPC1_LA28_N	LVDS	AL36
G36	FMC_HPC1_LA33_P	LVDS	AG32	H34	FMC_HPC1_LA30_P	LVDS	AJ30
G37	FMC_HPC1_LA33_N	LVDS	AG33	H35	FMC_HPC1_LA30_N	LVDS	AJ31
G39	VADJ_1V8_FPGA			H37	FMC_HPC1_LA32_P	LVDS	AG31
				H38	FMC_HPC1_LA32_N	LVDS	AH31
				H40	VADJ_1V8_FPGA		

Table 1-35: **J2 VITA 57.1 FMC HPC1 Connections *(Cont'd)***

J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J2 FMC HPC1 Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J/K Connections to FPGA U1							
J2	NC	NA	NA	K1	NC	NA	NA
J3	NC	NA	NA	K4	NC	NA	NA
J6	NC	NA	NA	K5	NC	NA	NA
J7	NC	NA	NA	K7	NC	NA	NA
J9	NC	NA	NA	K8	NC	NA	NA
J10	NC	NA	NA	K10	NC	NA	NA
J12	NC	NA	NA	K11	NC	NA	NA
J13	NC	NA	NA	K13	NC	NA	NA
J15	NC	NA	NA	K14	NC	NA	NA
J16	NC	NA	NA	K16	NC	NA	NA
J18	NC	NA	NA	K17	NC	NA	NA
J19	NC	NA	NA	K19	NC	NA	NA
J21	NC	NA	NA	K20	NC	NA	NA
J22	NC	NA	NA	K22	NC	NA	NA
J24	NC	NA	NA	K23	NC	NA	NA
J25	NC	NA	NA	K25	NC	NA	NA
J27	NC	NA	NA	K26	NC	NA	NA
J28	NC	NA	NA	K28	NC	NA	NA
J30	NC	NA	NA	K29	NC	NA	NA
J31	NC	NA	NA	K31	NC	NA	NA
J33	NC	NA	NA	K32	NC	NA	NA
J34	NC	NA	NA	K34	NC	NA	NA
J36	NC	NA	NA	K35	NC	NA	NA
J37	NC	NA	NA	K37	NC	NA	NA
J39	NC	NA	NA	K38	NC	NA	NA
				K40	NC	NA	NA

Notes:

1. Series capacitor coupled to the XCVU095 U1 pin.
2. U30 MAX15301 VADJ_1V8_FPGA voltage regulator power good output signal.
3. FPGA U1 JTAG TCK, TMS, TDO pins AE13, AF15, AD13 buffered by U19 SN74AVC8T245.
4. J2 HPC1 TDO-TDI connections to U132 HPC1 FMC JTAG bypass switch (N.C. normally closes/bypassing J2 until an FMC card is plugged into J2).
5. FMC_HPC1_PRSNT_M2C_B is the HPC1 FMC JTAG bypass switch U132.4 OE control signal and is also connected to the FPGA U1 pin BD23 via level shifter U44.
6. Connected to the FPGA U1 LS pins AP21/AN21 IIC_MAIN_SDA/SCL via IIC MUX U80 and level shifter U77.
7. HPC1 FMC signal FMC_HPC1_PG_M2C is connected to the FPGA U1 pin AU24 via level shifter U44.

VCU108 Board Power System

The VCU108 hosts a Maxim PMBus based power system. Figure 1-29 shows the VCU108 power system block diagram.

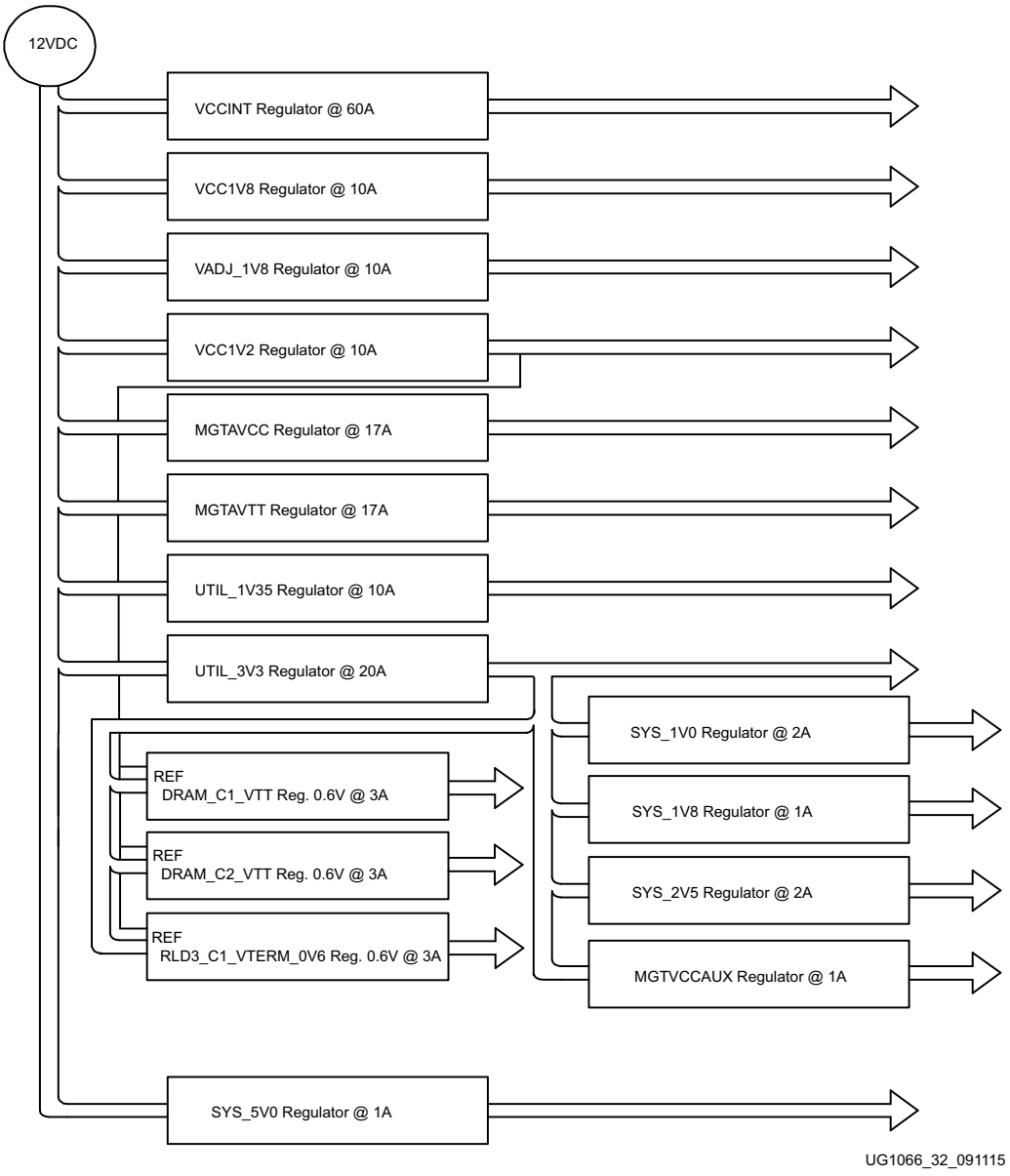


Figure 1-29: **VCU108 Power System Block Diagram**

The VCU108 evaluation board uses power regulators and PMBus compliant PoL controllers from Maxim Integrated Circuits to supply the core and auxiliary voltages listed in Table 1-36.

Table 1-36: **Onboard Power System Devices**

Device Type	Reference Designator	PMBus Address	Description	Power Rail Net Name	Power Rail Voltage
MAX20751EKX	U164	0x70	Maxim multiphase master with smart slaves VT1697SBFQX 60A	VCCINT_FPGA	0.95V
MAX15301	U9	0x11	Maxim InTune digital POL controller 10A	VCC1V8_FPGA	1.80V
MAX15301	U30	0x12	Maxim InTune digital POL controller 10A	VADJ_1V8_FPGA	1.80V
MAX15301	U4	0x14	Maxim InTune digital POL controller 10A	VCC1V2_FPGA	1.20V
MAX20751EKX	U166	0x72	Maxim multiphase master with smart slave VT1697SBFQX 17A	MGTAVCC_FPGA	1.00V
MAX20751EKX	U165	0x73	Maxim multiphase master with smart slave VT1697SBFQX 17A	MGTAVTT_FPGA	1.20V
MAX8869EUE	U167	NA	Maxim fixed LDO 1A	MGTVCCAUX	1.80V
MAX15301	U150	0x1A	Maxim InTune digital POL controller 10A	UTIL_1V35	1.35V
MAX15301	U156	0x1B	Maxim InTune digital POL controller 20A	UTIL_3V3	3.30V
MAX17502	U82	NA	Maxim synchronous buck switcher 1A	SYS_5V0	5.00V
MAX15053	U124	NA	Maxim adjustable synchronous buck switcher 2A	SYS_1V0	1.00V
MAX15027	U125	NA	Maxim adjustable LDO 1A	SYS_1V8	1.80V
MAX15053	U151	NA	Maxim adjustable synchronous buck switcher 2A	SYS_2V5	2.50V
TPS51200	U24	NA	TI source-sink V_{TT} regulator 3A	DDR4_C1_VTT	0.60V
TPS51200	U134	NA	TI source-sink V_{TT} regulator 3A	DDR4_C2_VTT	0.60V
TPS51200	U143	NA	TI source-sink V_{TT} regulator 3A	RLD3_C1_VTERM	0.60V

Documentation describing PMBus programming for the Maxim multiphase master and InTune power controllers is available at the Maxim website [Ref 29]. The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583) [Ref 30].

FMC VADJ_1V8 Power Rail

The VCU108 evaluation board implements the ANSI/VITA 57.1 section 5.5.1 IPMI support functionality. The power control of the VADJ_1V8 power rail is significantly different from other Xilinx evaluation boards, and is managed by the U111 system controller. This rail powers both the FMC HPC0 (J22) and the FMC HPC1 (J2) VADJ pins, as well as the XCVU095 HP banks 47, 48, 66, 67, and 68 (see Table 1-3). The valid values of the VADJ_1V8 rail are 1.2V, 1.5V, and 1.8V.

At power on, the system controller detects if an FMC module is connected to each interface:

- If no cards are attached to the FMC ports, the VADJ voltage is set to 1.8V.
- When one FMC card is attached, its IIC EEPROM is read to find a VADJ voltage supported by both the VCU108 board and the FMC module, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- When two FMC cards are attached with differing VADJ requirements, VADJ_1V8 is set to the lowest value compatible with the VCU108 board and the FMC modules, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- If no valid information is found in the IIC EEPROM, the VADJ_1V8 rail is set to 0.0V.

The system controller user interface (see FMC Menu Options in Appendix C) allows the FMC IPMI routine to be overridden and an explicit value can be set for the VADJ_1V8_FPGA rail.

Monitoring Voltage and Current

Voltage and current monitoring and control for the Maxim power system is available through either the VCU108 system controller or via the Maxim PowerTool software GUI.

The VCU108 system controller is the simplest and most convenient way to monitor the voltage and current values for the power rails listed in Table 1-36. For details on how to use this built-in feature see PMBus Menu and SYSMON Menu in Appendix C.

The Maxim power controllers listed in Table 1-36 can also be accessed through the PMBus connector J39. Using this connector requires the Maxim PowerTool USB cable (Maxim part number MAXPOWERTOOL002#). This cable can be ordered from the Maxim Integrated website [Ref 29]. The associated Maxim PowerTool GUI is also downloadable from the Maxim website.

SYSMON Power System Measurement

UltraScale FPGAs provide an analog converter (SYSMON) block. The SYSMON block contains a single 10-bit 0.2 MSPS ADC. The VCU108 board SYSMON ADC interface includes current measuring capability for all FPGA voltage rails. The rail current measurements are made available to SYSMON via an Analog Devices ADG707BRU multiplexer U75. Each rail has a TI INA333 op amp strapped across a series current sense resistors' Kelvin terminals.This op amp has its gain adjusted to give 0.75V – 1V at the expected full scale current value for the rail. The SYSMON block can measure the internal VCCINT, VCCAUX, and VCCBRAM rail voltages and the external MGTAVCC and MGTAVTT rail voltages using SYSMON channels AD0 and AD8, respectively.

Figure 1-30 shows the SYSMON external multiplexer U75 circuit block diagram.

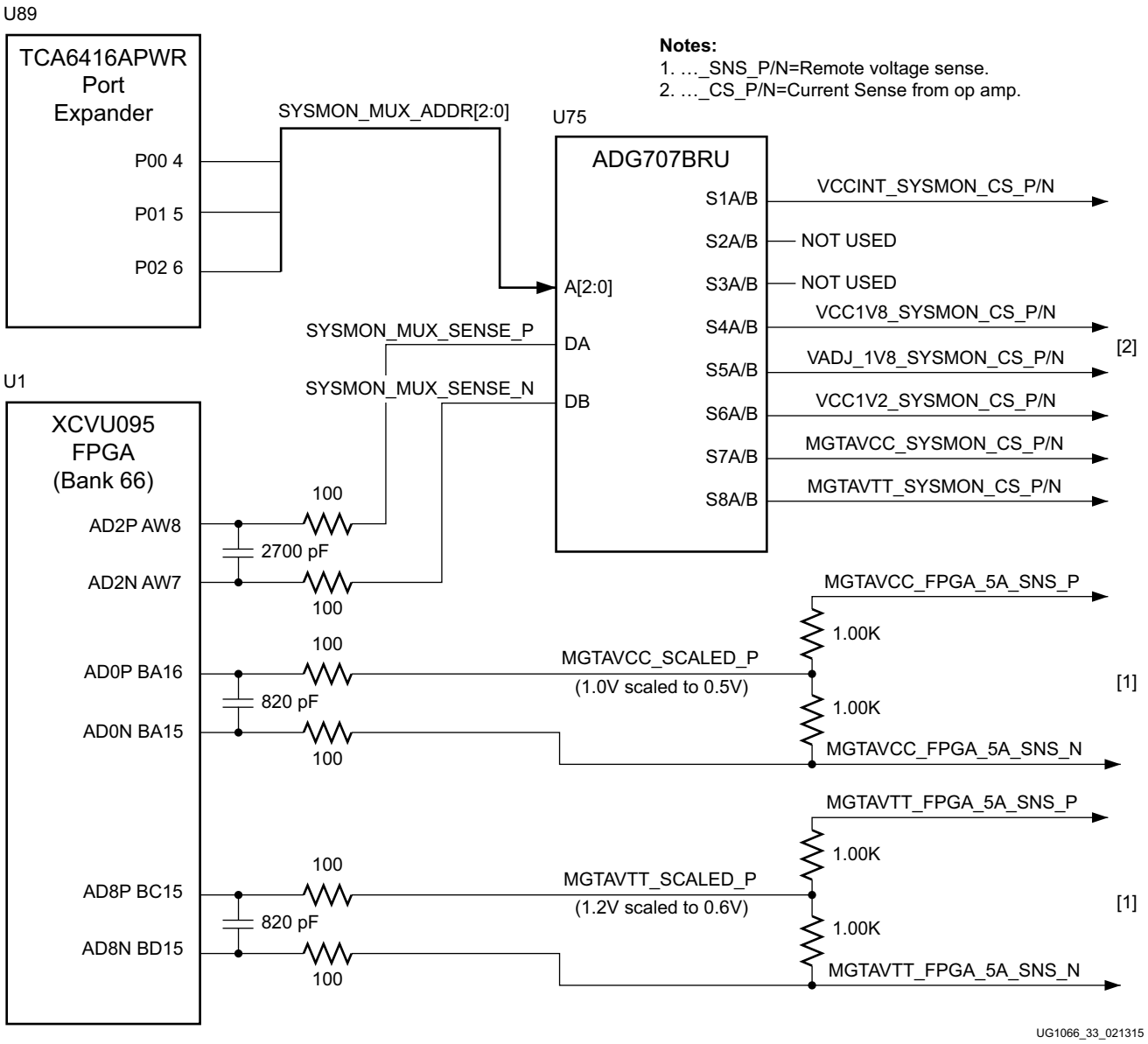


Figure 1-30: **SYSMON External Multiplexer Block Diagram**

Table 1-37 lists the VCU108 board SYSMON power system voltage and current measurement details for the external U75 MUX.

Table 1-37: **SYSMON Measurements through MUX U75**

Controlled Rail Name	Regulator Reference Descriptor	Measurement Type	Nominal V_{OUT}	Current Range	I_{SENSE} Op Amp			Schematic Net Name	8-to-1 MUX U75		
					Reference Designator	Gain	V_O Range		Pin Number	Pin Name	A[2:0]
VCCINT_FPGA	U164	V	0.95V	N/A	N/A			SYSMON or MAXIM GUI	N/A		
		I	N/A	0-60A	U74	15	0-1V	VCCINT_SYSMON_CS_P	19	S1A	000
								VCCINT_SYSMON_CS_N	11	S1B	
VCC1V8_FPGA	U9	V	1.80V	N/A	N/A			MAXIM GUI ONLY	N/A		
		I	N/A	0-10A	U116	20	0-1V	VCC1V8_SYSMON_CS_P	22	S4A	011
								VCC1V8_SYSMON_CS_N	8	S4B	
VADJ_1V8_FPGA	U30	V	1.80V	N/A	N/A			MAXIM GUI ONLY	N/A		
		I	N/A	0-10A	U119	20	0-1V	VADJ_1V8_SYSMON_CS_P	23	S5A	100
								VADJ_1V8_SYSMON_CS_N	7	S5B	
VCC1V2_FPGA	U4	V	1.20V	N/A	N/A			MAXIM GUI ONLY	N/A		
		I	N/A	0-10A	U120	20	0-1V	VCC1V2_SYSMON_CS_P	24	S6A	101
								VCC1V2_SYSMON_CS_N	6	S6B	
MGTAVCC_FPGA	U166	V	1.00V	N/A	N/A			SYSMON AD0 or MAXIM GUI	N/A		
		I	N/A	0-17A	U118	54.4	0-1V	MGTAVCC_SYSMON_CS_P	25	S7A	110
								MGTAVCC_SYSMON_CS_N	5	S7B	
MGTAVTT_FPGA	U165	V	1.20V	N/A	N/A			SYSMON AD8 or MAXIM GUI	N/A		
		I	N/A	0-17A	U117	54.4	0-1V	MGTAVTT_SYSMON_CS_P	26	S8A	111
								MGTAVTT_SYSMON_CS_N	4	S8B	

SYSMON Headers J80, J81

UltraScale FPGAs provide an analog front end (SYSMON) block. The SYSMON contains a single 10-bit 0.2 MSPS ADC. Consequently, the sequencer for SYSMON does not support simultaneous sampling mode or independent ADC mode. See the *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 31] for details on the capabilities of the analog front end.

The VCU108 board supports both the internal FPGA sensor measurements and the external measurement capabilities of the SYSMON. Internal measurements of the die temperature, VCCINT, VCCAUX, and VCCBRAM are available.

For external measurements SYSMON headers (J80, J81) are provided to connect analog inputs to the FPGA bank 0 dedicated VP/VN input channel. For more detailed information about the UltraScale System Monitor (SYSMON), see *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 31].

Cooling Fan

The XCVU095 FPGA U1 cooling fan connector is shown in Figure 1-31.

The fan turns on when the VCU108 is powered up due to pull-up resistor R422. The SM_FAN_PWM and SM_FAN_TACH signals are wired to the XCVU095 FPGA U1 bank 65 pins BF21 and BE17, respectively, enabling the implementation of a fan speed control IP in the FPGA U1 logic.

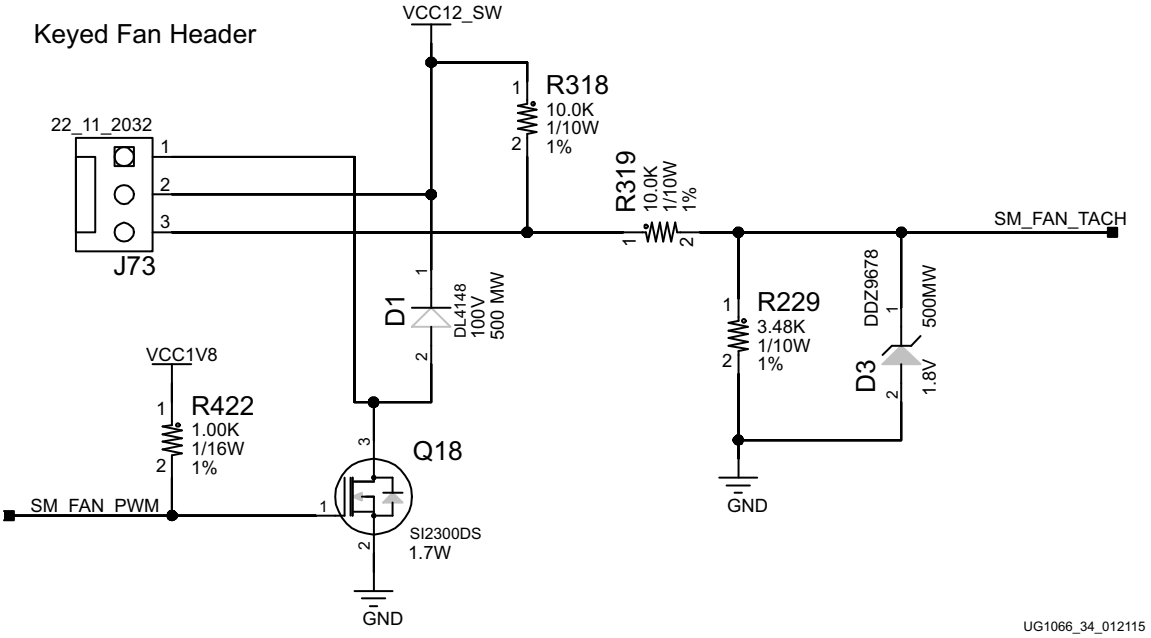


Figure 1-31: **Cooling Fan Circuit**

VCU108 Zynq-7000 SoC XC7Z010 System Controller

[Figure 1-2, callout 36]

The VCU108 XC7Z010 U111 system controller sub-system implements interfaces to:

- PMBus power system
- Programmable user clock
- Micro-SD card
- USB UART2
- Five directional user pushbutton switches
- I2C bus MUXes

The system controller is delivered as a black-box design that communicates with onboard programmable devices over an I2C interface. The Zynq-7000 SoC system controller IP is not provided and is not available to end users for modification purposes.

The system controller is an ease-of-use feature that sets up or queries onboard resources available to the XCVU095 UltraScale FPGA U1 on the VCU108. Programmable clocks, the internal UltraScale FPGA system monitor block (SYSYMONE1), and the Maxim power controllers are accessible through an I2C interface connected to both the system controller and the FPGA.

A Silicon Labs Si570 programmable low-jitter clock is used to provide a system clock for FPGA designers. Using a UART (115200-8-N-1) text interface, the system clock (Si570) can be set to any frequency between 10 MHz and 810 MHz. The Si570 defaults to a power-on frequency of 156.25 MHz, but then automatically changes to the last saved frequency setting if the system controller frequency auto-restore feature has been configured to ON for this clock. Refer to Option 6: View VCU108 Clocks Restore Options in Appendix C for information on how to enable this feature. Clock programming does not require FPGA resources and can be set or adjusted prior to configuring the FPGA or after the FPGA has been configured.

Additional functionality provided through the system controller UART2 includes a text display of the internal SYSMON registers for VCCINT, VCCBRAM, and VCCAUX, and the UltraScale FPGA U1 device temperature. SYSMON based power measurements are also displayed over the UART2 for the VCCINT, VCC1V8, VADJ_1V8, VCC1V2, MGTAVCC, and MGTAVTT power rails.

Power rail voltages set by the Maxim controllers are also displayed through the UART2 for VCCINT, VCCBRAM, VCCAUX, VCC1V8, VADJ_1V8, VCC1V2, MGTAVCC, MGTAVTT, MGTVCCAUX, and UTIL_3V3.

Appendix C, System Controller describes the system controller menus and options available through a PC-hosted terminal utility.

Configuration Options

The VCU108 board supports two of the five UltraScale FPGA configuration modes:

- Master BPI using the onboard linear BPI flash memory
- JTAG using:
  - USB JTAG configuration port (Digilent module U115)
  - Xilinx platform cable 2 mm, keyed flat cable header (J3)
  - * System controller from SD card

See *UltraScale Architecture Configuration User Guide* (UG570) [Ref 2] for further details on configuration modes.

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-38. The mode switches M2, M1, and M0 are on SW16 positions 3, 4, and 5, respectively. The FPGA default mode setting M[2:0] = **101**, selecting the JTAG configuration mode.

Table 1-38: **VCU108 Board FPGA Configuration Modes**

Configuration Mode	SW16 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master BPI	010	x8, x16	Output
JTAG	101	x1	Not applicable

Figure 1-32 shows mode switch SW16.

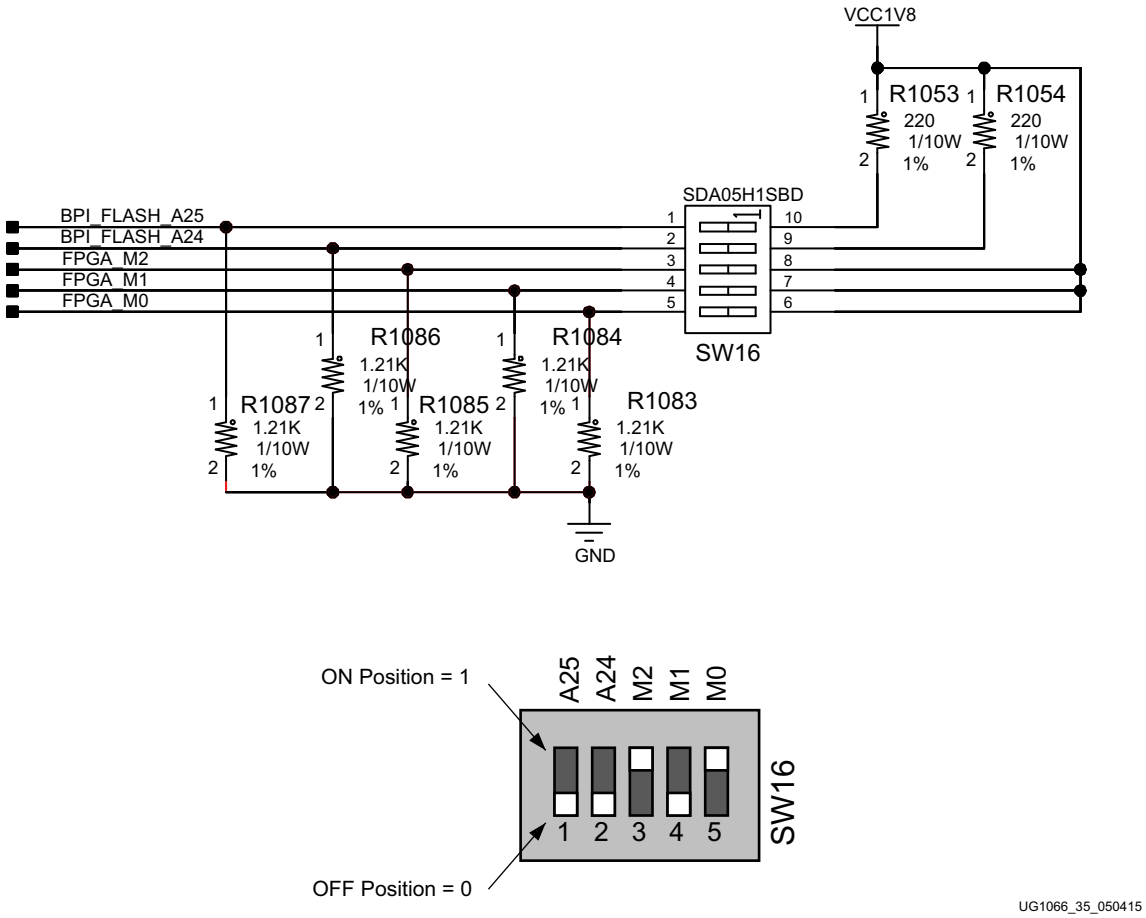


Figure 1-32: **SW16 Default Settings**

The mode pins settings on SW16 determine if the linear BPI flash is used for configuring the FPGA. DIP switch SW16 also provides the upper two address bits for the linear BPI flash and can be used to select one of multiple stored configuration bitstreams.

To obtain the fastest configuration speed, an external 90 MHz clock from the Silicon Labs Si5335A U122 is wired to the EMCCLK pin of the FPGA on bank 65 pin AL20. This allows the creation of bitstreams to configure the FPGA over the 16-bit datapath from the linear BPI flash memory at a maximum synchronous read rate of 90 MHz.

Appendix A

Default Switch and Jumper Settings

The default switch and jumper settings for the VCU108 evaluation board are provided in this appendix.

Switches

Default switch settings are listed in Table A-1.

Table A-1: **Default Switch Settings**

Switch	Function	Default	Comments	Figure 1-2 Callout	Schematic 0381556 Page
SW1	SPST slide switch	OFF	Board shipped with power switch off	30	71
SW12	4-Pole GPIO dip(1)	0000	Positions 1-4, GPIO active-High	26	61
SW15	5-Pole configuration dip(1)	00000	Positions 1-5, Zynq-7000 SoC system controller U111	28	51
SW16	5-Pole configuration dip(1)	00101	Positions 3-5, FPGA U1 mode M[2:0]	35	3

Notes:

1. DIP switches are active-High (connected net is pulled high when DIP switch is closed).

Jumpers

Default jumper positions are listed in Table A-2. See Figure Figure A-1 for locations of jumpers listed in Table A-2.

Table A-2: **Default Jumper Settings**

Jumper	Function	Default	Comments	Figure 1-2 Callout	Schematic 0381556 Page
J5	POR override	2-3	U1 POR_OVERRIDE pin P7 to GND	1	3
J12	Maxim regulator inhibit	Off	Used when programming PWR.SYS.	2	71
J14	U30 VADJ_1V8 enable	Off	Parallel to J12 VADJ_1V8 enable	3	74
J74	PCIe lane size select	5-6	8-lane configuration	4	45
J80	SYSMON_VP	1-2	U1 VP pin V12 pull down 20.5K to GND	5	3
J81	SYSMON_VN	1-2	U1 VN pin W11 pull down 20.5K to GND	6	3

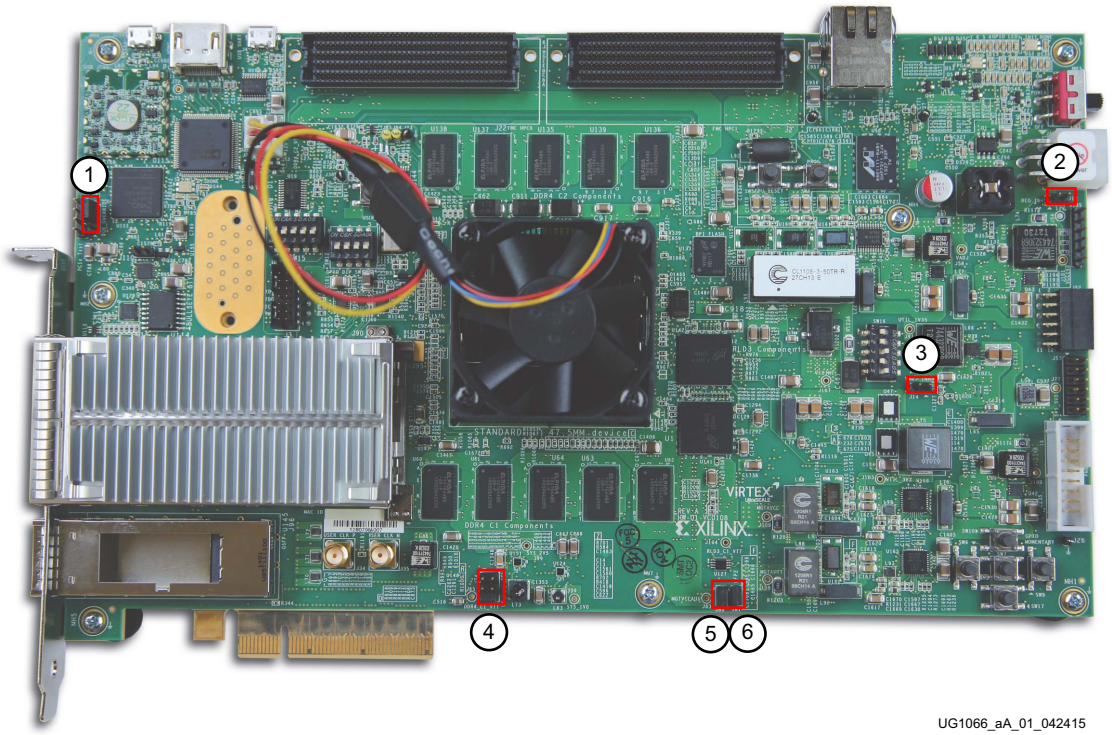


Figure A-1: **VCU108 Board Jumper Header Locations**

VITA 57.1 FMC Connector Pinouts

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) connector defined by the VITA 57.1 FMC specification. For a description of how the VCU108 evaluation board implements the FMC specification, see the FPGA Mezzanine Card Interface section.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG1065_aB_01_062615

Figure B-1: **FMC Connector Pinouts**

Appendix C

System Controller

Overview

The Xilinx system controller is an ease-of-use application that runs on a Zynq-7000 SoC at power-up on all UltraScale FPGA evaluation boards. These select board features can be controlled and monitored:

- Programmable clocks
- Power system monitoring (PMBus)
- UltraScale FPGA system monitor (SYSMON)
- Adjustable FMC expansion interface voltage
- GPIO pushbuttons and configuration DIP switch
- UltraScale FPGA Configuration

On power-up, the system controller presents a menu-driven selection of actions invoked by running a terminal program over a UART (115200-8-N-1) connection through the USB-to-UART bridge interface (J4).

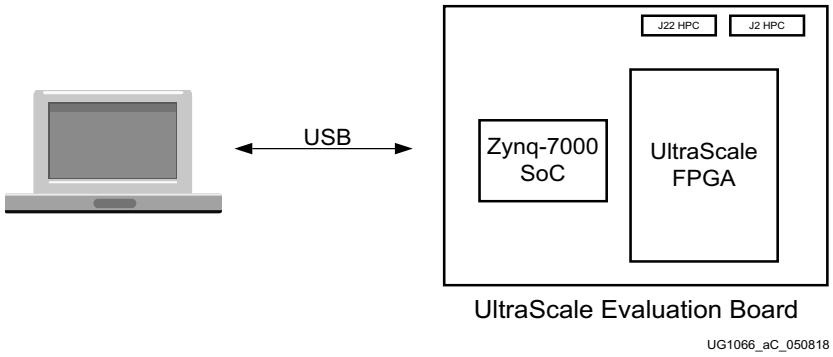


Figure C-1: **PC Host (Terminal Window) and UltraScale Evaluation Board**

System Controller Menu

Access the system controller menu as follows:

1. Install the Silicon Labs CP2105GM dual USB-to-UART bridge driver by following the instructions in the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033) [Ref 32].
2. The Tera Term terminal application installation is referenced in the driver installation instructions in step 1, which point to the *Tera Term Terminal Emulator Installation Guide* (UG1036) [Ref 33].
3. With the VCU108 evaluation board power turned off, install the USB cable supplied in the VCU108 evaluation board kit (standard type-A end to host computer, type Micro-B end to VCU108 evaluation board connector J4).
4. Turn on the VCU108 evaluation board. The PC recognizes that new hardware is connected, and runs the driver installation wizard to complete the installation of the CP2015GM bridge chip drivers. The system controller UART appears in the PC device manager ports (COM &LPT) list as the Silicon Labs Dual CP210x Enhanced COM Port (COMnn).
5. Open a Tera Term terminal window on the PC desktop. In the New connection dialog box, click the serial radio button, and then click the drop-down arrow to open the list of ports. Select the COM port with the Enhanced description. Click OK.
6. At the top of the Tera Term VT window, select Setup > Serial port. In the dialog box that appears, set baud rate to 115200, data to 8 bit, parity to none, stop to 1 bit, and flow control to none. Click OK.
7. Power cycle the VCU108 evaluation board. The Tera Term window displays the VCU108 evaluation board system controller main menu.

The main menu lists seven sub-menus that carry out selected actions.

```
VCU108 System Controller
- Main Menu-
1. Set Programmable Clocks (see Clock Menu)
2. Get Power System (PMBus) Voltages (see PMBus Menu)
3. Get UltraScale FPGA System Monitor (SYSMON) Data (see SYSMON Menu)
4. Adjust FPGA Mezzanine Card (FMC) Settings (see FMC Menu)
5. Get GPIO Data (see GPIO Menu)
6. Get EEPROM Data (see EEPROM Menu)
7. Configure UltraScale FPGA (see CONFIG Menu)
Select an option
```

The menu system is shown in Figure C-2.

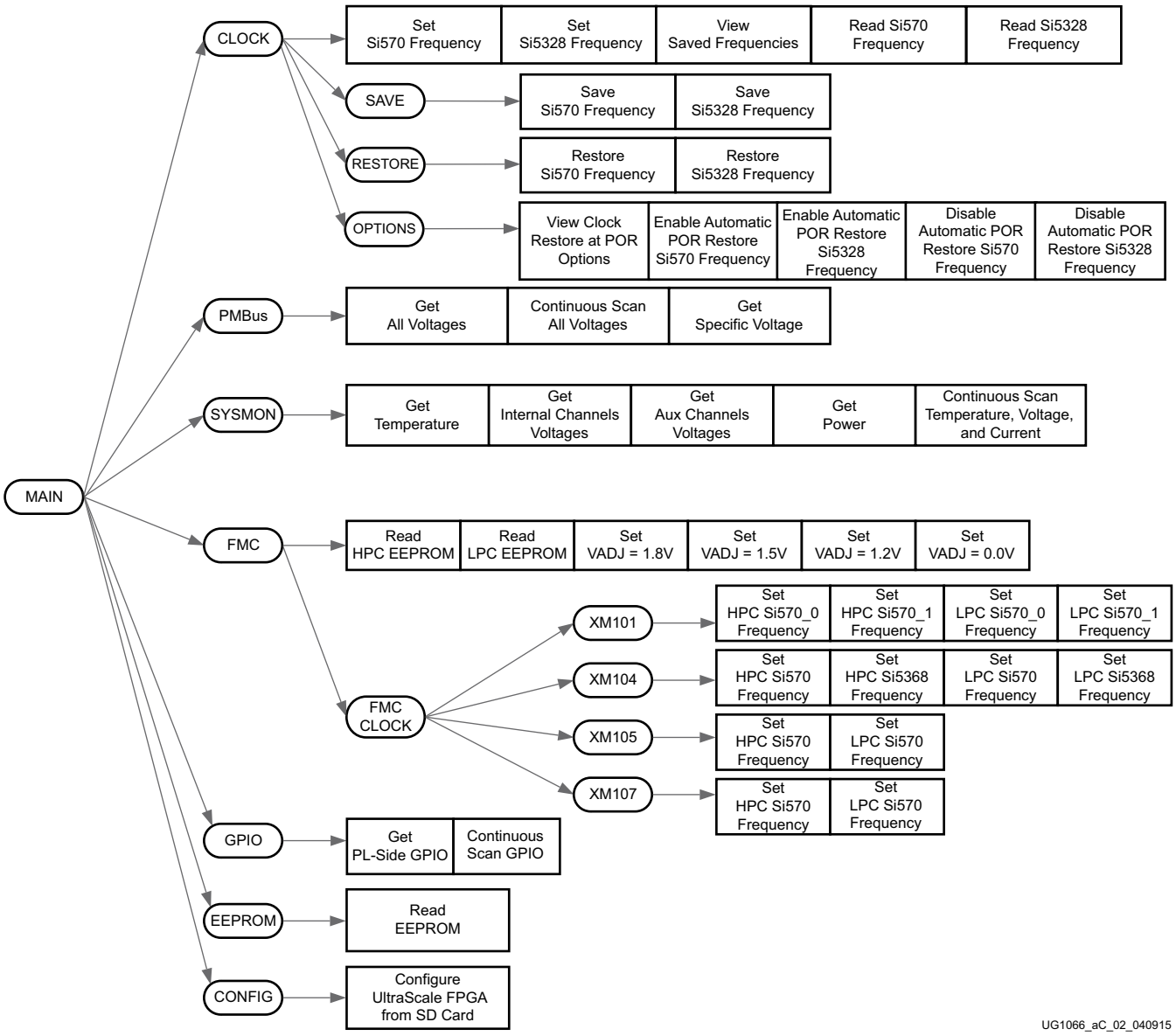


Figure C-2: **System Controller Menu System**

Power-On and Reset

Prior to displaying the main menu, the system controller initializes the adjustable voltage (VADJ) on the FPGA FMC expansion port interface within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.

- If no cards are attached to the FMC ports, the VADJ voltage is set to 1.8V.
- When one FMC card is attached, its I2C EEPROM is read to find a VADJ voltage supported by both the VCU108 board and the FMC module within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.
- When two FMC cards are attached with differing VADJ requirements, VADJ is set to the lowest value compatible with the VCU108 board and the FMC modules, within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V.

The VADJ voltage is set and then the main menu is displayed. The VADJ settings can be viewed by scrolling back through the terminal window output.

IMPORTANT: *If an attached FMC card does not have its I2C EEPROM programmed, the firmware sets VADJ to 0.0V.*

The VADJ voltage can be set manually with the FMC menu.

VCU108 On-board Clocks

The VCU108 board hosts two programmable clocks. One is the user programmable system clock (Silicon Labs Si570) that operates in the frequency range between 10 MHz and 810 MHz. The second VCU108 programmable clock source is the Silicon Labs Si5328B, which is typically used as a jitter attenuator for a recovered clock from a serial transceiver. However, the Si5328B can also be used as an independent clock source with a frequency range of 8 kHz to 808 MHz. In addition to the programmable clock sources, the UltraScale FPGA evaluation boards provide a 300 MHz fixed frequency system clock.

Clock Menu

The clock menu is used to set the frequency of the onboard programmable clock sources. At VCU108 board power-up, the onboard programmable clock sources generate their factory default frequencies until the system controller has booted and checked the onboard EEPROM to determine if a frequency value has previously been saved for either onboard clock source. Previously saved values are restored to the onboard clock sources, which then output these frequencies until they are reprogrammed to a different value, or the VCU108 board is turned off.

A VCU108 board power cycle (power off/power on) returns the clock sources to the factory default settings. On the UltraScale FPGA evaluation boards, the factory default for the Si570 is 156.250 MHz, and the factory default for the Si5328 is 0 Hz.

The programmable clock frequencies of the VCU108 board can be set and saved for later restoration. The saved frequencies are maintained in the VCU108 board onboard non-volatile I2C EEPROM. The clock menu is used to manually restore previously saved clock frequencies.

This section includes a description of the clock menu options, presenting arbitrary sample value entries and the system controller responses. The entry value commentary is shown in parentheses.

```
VCU108 System Controller
- Clock Menu-
1. Set VCU108 Si570 User Clock Frequency
2. Set VCU108 Si5328 MGT Clock Frequency
3. Save VCU108 Clock Frequency to EEPROM
4. Restore VCU108 Clock Frequency from EEPROM
5. View VCU108 Saved Clocks in EEPROM
6. Set VCU108 Clock Restore Options
7. Read VCU108 Si570 User Clock Frequency
8. Read VCU108 Si5328 MGT Clock Frequency
0. Return to Main Menu
Select an option
```

Clock Menu Options

Option 1: Set VCU108 Si570 User Clock Frequency

```
Enter the Si570 frequency <10-810MHz>:
```

(enter a value between 10 and 810)

```
100

RFreq_Cal[0]=0x02,RFreq_Cal[1]=0xBC,RFreq_Cal[2]=0x00,RFreq_Cal[3]=0xE4,
RFreq_Cal[4]=0xED
Freq: 100.0000000000 HS_DIV=5 N1=10 DCO=5000.0 RFREQ= 0x02BC00E4ED
```

(The returned values include configuration setting details.)

Option 2: Set VCU108 Si5328 MGT Clock Frequency

```
Enter the Si5328 frequency (0.008-808MHz):
```

200

IMPORTANT: *Several seconds might elapse before the result is returned.*

```
Freq:200.0000000000 fosc=5600.000MHz f3=5.000KHz LBW=0.200KHz N1=28 N1_HS=7
NC1_LS=4 N2=1120000 N2_HS=4 N2_LS=280000 N31=40000 N32=22857
```

(The returned values include configuration setting details.)

Option 3: Save VCU108 Clock Frequency to EEPROM

```
VCU108 System Controller
        - Save Menu -
----------------------------
1. Save VCU108 Si570 Frequency to EEPROM
2. Save VCU108 Si5328 Frequency to EEPROM
0. Return to Clock Menu
Select an option
```

- Save VCU108 Si570 Frequency to EEPROM

  ```
  Saving Si570 Frequency = 200.000 to EEPROM
  ```

- Save VCU108 Si5328 Frequency to EEPROM

  ```
  Saving Si5328 Frequency = 150.000 to EEPROM
  ```

- Return to Clock Menu

  This option returns to the menu level above.

Option 4: Restore VCU108 Clock Frequency from EEPROM

If either clock device is reprogrammed and the frequency value is not saved, the previously saved frequency can be restored to the clock source.

```
VCU108 System Controller
     - Restore Menu -
----------------------------
1. Restore VCU108 Si570 Frequency from EEPROM
2. Restore VCU108 Si5328 Frequency from EEPROM
0. Return to Clock Menu
Select an option
```

- Restore VCU108 Si570 Frequency from EEPROM

```
Freq:200.0000000000 HS_DIV=7 N1=4 DCO=5600.0 RFREQ=0x030FFF204B
Restored Si570 Frequency = 200.000 from EEPROM
```

  (The returned values include configuration setting details.)

- Restore VCU108 Si5328 Frequency from EEPROM

```
Restoring Si5328 Frequency = 150.000 from EEPROM
Freq:150.0000000000 fosc=5400.000MHz f3=15.000KHz LBW=0.600KHz N1=36 N1_HS=6
NC1_LS=6 N2=360000 N2_HS=4 N2_LS=90000 N31=10000 N32=7619
```

  (The returned values include configuration setting details.)

- Return to Clock Menu

  This option returns to the menu level above.

Option 5: View VCU108 Saved Clocks in EEPROM

This option is for verifying that the recently programmed values are in EEPROM.

```
Saved Clocks in EEPROM
------------------------------
Si570 User Clock: 200.00000000 MHz
Si5328 MGT Clock: 150.00000000 MHz
```

Option 6: View VCU108 Clocks Restore Options

```
VCU108 System Controller
- Options Menu-
-----------------------------------------------
1. View VCU108 Clock Restore Options
2. Enable VCU108 Si570 Automatic Restore at Power-Up Reset
3. Enable VCU108 Si5328 Automatic Restore at Power-Up Reset
4. Disable VCU108 Si570 Automatic Restore at Power-Up Reset
5. Disable VCU108 Si5328 Automatic Restore at Power-Up Reset
0. Return to Clock Menu
Select an option
```

- View VCU108 Clock Restore Options

```
Clock Restore Options:
-----------------------------------------------
Si570 Automatic Restore at Power-Up Reset = DISABLED
Si5328 Automatic Restore at Power-Up Reset = DISABLED
```

- Enable VCU108 Si570 Automatic Restore at Power-Up Reset

  There is no menu response to selecting this option. To verify that the enabling function occurred, select option 1 again.

- Enable VCU108 Si5328 Automatic Restore at Power-Up Reset

  There is no menu response to selecting this option. To verify that the enabling function occurred, select option 1 again.

- View VCU108 Clock Restore Options

```
 Clock Restore Options:
---------------------------------------------
Si570 Automatic Restore at Power-Up Reset = ENABLED
Si5328 Automatic Restore at Power-Up Reset = ENABLED
```

- Return to Clock Menu

  This option returns to the menu level above.

Option 7: Read VCU108 Si570 User Clock Frequency

This option displays the current frequency setting of the Si570.

```
Si570 Current Frequency = 1.562500E+02 MHz
```

Option 8: Read VCU108 Si5328 MGT Clock Frequency

This option displays the current frequency setting of the Si5328.

```
Si5328 CKOUT1 Current Frequency = 2.000000E+02 MHz
Si5328 CKOUT1 Current Frequency = 2.000000E+02 MHz
```

- Return to Main Menu

  This option returns to the menu level above.

PMBus Menu

The PMBus is an I2C bus that is used to read the voltage settings of the nine VCU108 power rails controlled by the Maxim power system. Through the PMBus menu these power rails can be read once or scanned continuously until stopped by a key press. Table C-1 lists the voltage rails accessible through the system controller's interface to the Maxim PMBus.

Table C-1: **Maxim Power Supply Rail**

Maxim Power Supply Rail	I2C Address	Nominal Voltage
VCCINT	0x0A	0.95V
VCC1V8	0x11	1.80V
VADJ_1V8	0x12	1.80V
VCC1V2	0x14	1.20V
MGTAVCC	0x72	1.00V
MGTAVTT	0x73	1.20V
UTIL_3V3	0x1B	3.30V
UTIL_1V35	0x1A	1.35V

PMBus Menu Options

```
VCU108 System Controller
- PMBus Menu-
1. Get PMBus Voltages
2. Continuous Scan PMBUS Voltages
3. Get VCCINT Voltage
4. Get VCC1V8 Voltage
5. Get VADJ1V8 Voltage
6. Get VCC1V2 Voltage
7. Get MGTAVCC Voltage
8. Get MGTAVTT Voltage
9. Get UTIL3V3 Voltage
A. Get UTIL1V35 Voltage
0. Return to Main Menu
Select an option
```

Option 1: Get PMBus Voltages

```
VCCINT, VCCBRAM    = 0.950V
VCCAUX, VCC1V8     = 1.800V
VCCBRAM, VCCINT    = 0.950V
VCC1V8, VCCAUX     = 1.800V
VADJ1V8            = 1.800V
```

```
VCC1V2              = 1.202V
MGTAVCC             = 1.000V
MGTAVTT             = 1.200V
UTIL3V3             = 3.299V
UTIL1V35            = 1.352V
```

Option 2: Continuous Scan PMBUS Voltages

The list of voltages shown in option 1 is displayed and updated about once per second. Pressing any key re-displays the PMBus menu.

Option 3: Get VCCINT Voltage

```
VCCINT = 0.950V (one-time snapshot of the VCCINT voltage)
Unscaled Hex: MSB = 0x0F, LSB = 0x34
```

(The returned values include configuration setting details.)

Option 4: Get VCC1V8 Voltage

```
VCC1V8 = 1.800V
Unscaled Hex: MSB = 0x1C, LSB = 0xCC
```

(The returned values include configuration setting details.)

Option 5: Get VADJ1V8 Voltage

```
VADJ1V8 = 1.800V
Unscaled Hex: MSB = 0x1C, LSB = 0xCB
```

(The returned values include configuration setting details.)

Option 6: Get VCC1V2 Voltage

```
VCC1V2 = 1.200V
Unscaled Hex: MSB = 0x13, LSB = 0x33
```

(The returned values include configuration setting details.)

Option 7: Get MGTAVCC Voltage

```
MGTAVCC = 1.000V
Unscaled Hex: MSB = 0x10, LSB = 0x00
```

(The returned values include configuration setting details.)

Option 8: Get MGTAVTT Voltage

```
MGTAVTT = 1.200V
Unscaled Hex: MSB = 0x13, LSB = 0x32
```

(The returned values include configuration setting details.)

Option 9: Get UTIL3V3 Voltage

```
UTIL3V3 = 3.299V
Unscaled Hex: MSB = 0x34, LSB = 0xC7
```

(The returned values include configuration setting details.)

Option A: Get UTIL1V35 Voltage

```
UTIL1V35 = 1.351V
Unscaled Hex: MSB = 0x15, LSB = 0x9F
```

(The returned values include configuration setting details.)

Option 0: Return to Main Menu

This option returns to the menu level above.

SYSMON Menu

The Virtex® UltraScale™ FPGA on the VCU108 contains a 200 KSPS analog-to-digital converter known as the system monitor (SYSMON), which is described in *UltraScale Architecture System Monitor User Guide (*UG580) [Ref 31]. Measurements made internal to the UltraScale FPGA are accomplished by the SYSMON block for VCCINT, VCCBRAM, and VCCAUX. In conjunction with an onboard analog multiplexer (Analog Devices ADG707) and inline Kelvin sense resistors, the UltraScale SYSMON ADC measures the current on the eight rails listed in Table C-2.

Table C-2: **SYSMON Monitored Power Rail**

SYSMON Monitored Power Rail	Nominal Voltage	Maximum Rail Current
VCCINT/VCCBRAM	0.95V	60A
VCC1V8/VCCAUX	1.80V	10A
VADJ_1V8	1.80V	10A
VCC1V2	1.20V	10A
MGTAVCC	1.00V	17A
MGTAVTT	1.20V	17A

The system controller reads and displays SYSMON based measurements prior to configuring the UltraScale FPGA. Bank 66 of the Virtex UltraScale device is the default SYSMON bank and is ready to monitor the SYSMON auxiliary channels at power-up. Auxiliary channels VAUX0, VAUX2, and VAUX8 are used to monitor MGTVCC, the ADG707 analog MUX, and MGTAVTT, respectively. At power-up, jumpers J80 and J81 connect SYSMON's VP and VN pins to ground, setting the default SYSMON I2C address to 0x32. This power-up default I2C address is used by the system controller to access SYSMON data.

If the VCU108 system controller SYSMON menu is used after the UltraScale FPGA has been configured with a design, the UltraScale resident design must contain logic to enable I2C access to the UltraScale system monitor and the internal (VCCINT, VCCBRAM, VCCAUX) and auxiliary channels (VAUX0, VAUX2, VAUX8). Designs that access I2C devices through the TCA9548 I2C switch must also deassert the TCA9548 reset pin from logic within the UltraScale FPGA. There is an external pull-up on this reset signal. See *UltraScale Architecture System Monitor User Guide (*UG580) [Ref 31] for more details.

Through the SYSMON menu, single readings or a continuous scan of the voltages, currents, power, and temperature are available. The minimum and maximum current usage for the monitored rails are also displayed and are reset each time the SYSMON menu is entered.

SYSMON Menu Options

```
VCU108 System Controller
- SYSMON Menu-
1. Get Temperature
2. Get Internal Channel Voltages
3. Get Auxiliary Channel Voltages
4. Get Power
5. Continuous Scan SYSMON Measurements
0. Return to Main Menu
Select an option
```

Option 1: Get Temperature

```
Temperature = 33.31 C Min = 30.65 C Max = 33.54 C
```

Option 2: Get Internal Channel Voltages

```
VCCINT  =  0.955V Max = 0.956V Min = 0.946V
VCCBRAM =  0.954V Max  = 0.954V Min = 0.945V
VCCAUX  =  1.804V Max = 1.805V Min = 1.796V
------------------
VPVN    = 0.003V
VREFP   = 1.257V
VREFN   = 0.012V
```

Option 3: Get Auxiliary Channel Voltages

```
VAUX_0 = 0.503V
VAUX_2 = 0.005V
VAUX_8 = 0.603V
```

Option 4: Get Power

```
-------------------------
VCCINT   POWER = 0.147 W
VCC1V8   POWER = 0.015 W
VADJ1V8  POWER = 0.089 W
VCC1V2   POWER = 0.068 W
MGTAVCC  POWER = 0.078 W
MGTAVTT  POWER = 0.035 W
-------------------------
```

Option 5: Continuous Scan SYSMON Measurements

```
Press Any Key to Return to SYSMON Menu
Temperature = 33.03 C Min = 30.51 C Max = 33.81 C
-----------------------------------------------------
                                        MIN       MAX
           Power    Voltage   Current   Current   Current
VCCINT:    0.30W    0.95V     0.31A     0.15A     0.37A
VCC1V8:    0.02W    1.80V     0.01A     0.01A     0.01A
VADJ_1V8:  0.06W    1.80V     0.03A     0.02A     0.06A
VCC1V2:    0.07W    1.20V     0.06A     0.05A     0.06A
MGTAVCC:   0.08W    1.00V     0.08A     0.07A     0.09A
MGTAVTT:   0.03W    1.20V     0.03A     0.02A     0.03A
```

Option 0: Return to Main Menu

This option returns to the menu level above.

FMC Menu

The VCU108 board provides two FMC ANSI/VITA 57.1 expansion interfaces that use a common VADJ voltage supply. At power-up, prior to displaying the main menu, the system controller initializes the VADJ on the FMC expansion port interface. If no cards are attached to the FMC ports, the VADJ voltage is set to 1.8V. Otherwise, the FMC module's I2C EEPROM is read to find a VADJ voltage supported by both the VCU108 board and the FMC module within the available choices of 1.8V, 1.5V, 1.2V, and 0.0V. The VADJ voltage is set and then

the main menu is displayed. Users can scroll back through their terminal window output and view the settings determined for VADJ. If an attached FMC card does not have its I2C EEPROM programmed, the VADJ voltage can be set manually with the FMC menu.

All FMC mezzanine cards must host an I2C EEPROM, powered from the always on 3P3VAUX rail, which can be read out through the FMC menu. A raw hexadecimal display and a formatted version of the FMC EEPROM data are provided through the FMC menu. The VITA 57.1 standard identifies the data fields of the intelligent platform management interface (IPMI) specification used for the FMC EEPROM. The VCU108 board system controller utilizes the board information area and the multi-record DC load record to query the FMC module for its VADJ requirements. See the VITA FMC Marketing Alliance website [Ref 28] for details on these standards. The VCU108 board system controller is aware of the programmable clock resources on these FMCs:

- FMC XM101 LVDS QSE card
- FMC XM104 MGT serial connectivity card
- FMC XM105 debug card
- FMC XM107 loopback card

These mezzanine cards can be attached to the J22 HPC or J2 HPC expansion ports on the VCU108 board. Table C-3 shows the accessible clock resources on each FMC module.

Table C-3: **FMC Module/Board**

Xilinx FMC Module/Board	Clock Source #1	Clock Source #2
XM101	Si570	Si570
XM104	Si570	Si5368
XM105	Si570	n/a
XM107	Si570	n/a
VCU108 Base Board	Si570	Si5328

FMC Menu Options

```
VCU108 System Controller
- FMC Menu-
1. Set FMC XMxxx CLOCKS
2. Read FMC HPC0 IIC EEPROM
3. Read FMC HPC1 IIC EEPROM
4. Set FMC VADJ to 1.8V
5. Set FMC VADJ to 1.5V
6. Set FMC VADJ to 1.2V
7. Set FMC VADJ to 0.0V
0. Return to Main Menu
Select an option
```

Identify the FMC module types plugged on to the VCU108 board, and which FMC connector is associated - the left J22 HPC or right J2 HPC. The examples shown in this section reflect the particular FMC installed at the VCU108 board J22 HPC FMC connector.

Option 1: Set FMC XMxxx CLOCKS

```
VCU108 System Controller
      - FMC Clock Menu -
----------------------------
1. Set FMC XM101 Clocks
2. Set FMC XM104 Clocks
3. Set FMC XM105 Clocks
4. Set FMC XM107 Clocks
0. Return to FMC Menu
Select an option
```

Set FMC XM101 Clocks

```
VCU108 System Controller
       - XM101 Menu -
----------------------------
1. Set HPC Si570_0 Frequency
2. Set HPC Si570_1 Frequency
3. Set LPC Si570_0 Frequency
4. Set LPC Si570_1 Frequency
0. Return to FMC Clock Menu
Select an option
```

- Set HPC Si570_0 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 31
Enter the Si570 frequency (10-810MHz):
50
```

```
Freq:50.0000000000 HS_DIV=7 N1=14 DCO=4900.0 RFREQ=0x02AE100C27
```

(The returned values include configuration setting details.)

- Set HPC Si570_1 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 31
Enter the Si570 frequency (10-810MHz):
100
Freq:100.0000000000 HS_DIV=5 N1=10 DCO=5000.0 RFREQ=0x02BC48225C
```

(The returned values include configuration setting details.)

- Return to FMC Clock Menu

This option returns to the menu level above.

Set FMC XM104 Clocks

```
VCU108 System Controller
      - XM104 Menu -
----------------------------
1. Set HPC Si570   Frequency
2. Set HPC Si5368 Frequency
3. Set LPC Si570   Frequency
4. Set LPC Si5368 Frequency
0. Return to FMC Clock Menu
Select an option
```

- Set HPC Si570 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 34
Enter the Si570 frequency (10-810MHz):
125
Freq:125.0000000000 HS_DIV=4 N1=10 DCO=5000.0 RFREQ=0x02BBEE4A63
```

(The returned values include configuration setting details.)

- Set HPC Si5368 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 34
Enter the Si5368 output frequency (0.002-808MHz):
205
```

IMPORTANT: *Several seconds may elapse before the result is returned.*

```
Freq:205.0000000000 fosc=4920.000MHz f3= 5.000KHz LBW=0.200KHz N1=24 N1_HS=6
NC1_LS=4 N2=984000 N2_HS=4 N2_LS=246000 N31=41000 N32=22857
```

(The returned values include configuration setting details.)

- Return to FMC Clock Menu

  This option returns to the menu level above.

Set FMC XM105 Clocks

```
VCU108 System Controller
      - XM105 Menu -
----------------------------
1. Set HPC0 Si570   Frequency
2. Set HPC1 Si570   Frequency
0. Return to FMC Clock Menu
Select an option
```

- Set HPC Si570 Frequency

  ```
  FMC HPC card present
  ```

  (The returned values include configuration setting details.)

  ```
  board_area_offset = 008
  board_area_format_version = 0x01
  board_area_length = 056
  board_mfg_hdr_offset = 014
  board_mfg_length = 010
  ReadBuffer index = 026
  ReadBuffer[i] = 58
  ReadBuffer[i+1] = 4D
  ReadBuffer[i+2] = 31
  ReadBuffer[i+3] = 30
  ReadBuffer[i+4] = 35
  Enter the Si570 frequency (10-810MHz):
  50
  Freq:50.0000000000 HS_DIV=7 N1=14 DCO=4900.0 RFREQ=0x02AE1505E5
  ```

  (The returned values include configuration setting details.)

- Return to FMC Clock Menu

  This option returns to the menu level above.

Set FMC XM107 Clocks

```
VCU108 System Controller
      - XM107 Menu -
----------------------------
1. Set HPC0 Si570   Frequency
2. Set HPC1 Si570   Frequency
0. Return to FMC Clock Menu
Select an option
```

- Set HPC Si570 Frequency

```
FMC HPC card present
```

(The returned values include configuration setting details.)

```
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 37
Enter the Si570 frequency (10-810MHz):
230
Freq:230.0000000000 HS_DIV=11 N1=2 DCO=5060.0 RFREQ=0x02C44FF69F
```

(The returned values include configuration setting details.)

- Return to FMC Clock Menu

  This option returns to the menu level above.

Return to FMC Menu

This option returns to the menu level above.

Option 2: Read FMC HPC0 IIC EEPROM

```
FMC HPC card present
```

The I2C EEPROM data displayed is too long to include in this appendix. If the FMC I2C EEPROM has been programmed, several data groupings are displayed:

ReadBuffer[000] - ReadBuffer[255] displays various value contents

```
Common Header
Board Area Info
MultiRecord Area
 - OEM FMC Record
 - DC Load Records (three groups)
 - DC Output Records (three groups)
If the FMC IIC EEPROM has not been programmed,
ReadBuffer[000] - ReadBuffer[255] displays buffer contents = 0xFF and
```

```
the Common Header reports "Invalid Format Version FF"
At the end of the displayed data, the system controller again displays the FMC Menu.
```

Option 3: Read FMC HPC1 IIC EEPROM

This option displays the FMC I2C EEPROM data, if programmed, in a similar fashion as option 2.

Options 4-7: Set FMC VADJ Voltage

Each of the following options sets the VADJ_1V8 rail to the voltage indicated. The result of choosing an option here may be viewed by returning to the Main Menu, choosing the SYSMON Menu, and selecting option 5: Continuous Scan SYSMON Measurements.

- Option 4: Set FMC VADJ to 1.8V
- Option 5: Set FMC VADJ to 1.5V
- Option 6: Set FMC VADJ to 1.2V
- Option 7: Set FMC VADJ to 0.0V

The result of choosing an option here can be viewed by returning to the Main Menu, choosing the SYSMON Menu, and selecting option 5: Continuous Scan SYSMON Measurements (the results after choosing option 5.Set FMC VADJ to 1.5V are shown here:

```
Press Any Key to Return to SYSMON Menu
Temperature = 33.29 C  Min = 28.15 C  Max = 33.96 C
-------------------------------------------------------
                                          MIN       MAX
           Power    Voltage   Current   Current   Current
VCCINT:    0.35W    0.95V     0.37A     0.17A     0.42A
VCCAUX:    0.42W    1.80V     0.23A     0.22A     0.24A
VCCBRAM:   0.05W    0.95V     0.05A     0.03A     0.05A
VCC1V8:    0.02W    1.80V     0.01A     0.01A     0.01A
VADJ_1V8:  0.06W    1.50V     0.04A     0.01A     0.06A
VCC1V2:    0.06W    1.20V     0.05A     0.05A     0.06A
MGTAVCC:   0.07W    1.00V     0.07A     0.07A     0.09A
MGTAVTT:   0.03W    1.20V     0.02A     0.02A     0.03A
```

Option 0: Return to Main Menu

This option returns to the menu level above.

GPIO Menu

The system controller continuously scans specific user activated inputs and several onboard status signals. Positions 1 – 4 (M3, M2, M1, M0) of MODE DIP switch SW15 are monitored, as well as the five directional user pushbuttons (N, S, E, W, C). The 4-position GPIO DIP switch SW12 is not monitored. The monitored onboard status signals include: FMC1_PRSNT, FMC2_PRSNT, PMBUS_CABLE_B, FPGA_IIC_BUSY, and PMBUS_ALERT.

GPIO Menu Options

```
VCU108 System Controller
- GPIO Menu-
1. Get GPIO PL Data
2. Continuous Scan GPIO Readings
0. Return to Main Menu
Select an option
```

Option 1: Get GPIO PL Data

```
----------------------
FMC1_PRSNT    = NO
FMC2_PRSNT    = YES
PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = NO
PMBUS_ALERT   = NO
```

Option 2: Continuous Scan GPIO Readings

```
Press any Key to Return to GPIO Menu
```

When any of the mode DIP SW15 poles 1-4 are changed, or a pushbutton pressed, the value beneath the switch position changes accordingly (showing a 0 or a 1).

```
SYS Mode DIP Switch (M3, M2, M1, M0)
                     0   0   0   0
Pushbuttons (N, S, E, W, C)
             0  0  0  0  0
----------------------
FMC1_PRSNT    = NO
FMC2_PRSNT    = YES
PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = NO
PMBUS_ALERT   = NO
```

Option 0: Return to Main Menu

This option returns to the menu level above.

EEPROM Menu

The system controller EEPROM menu is used to read the contents of the VCU108 on-board EEPROM.

EEPROM Menu Options

```
VCU108 System Controller
    - EEPROM Menu -
----------------------------
1. Read Board EEPROM Data
0. Return to Main Menu
Select an option
```

Option 1: Read Board EEPROM Data

```
EEPROM   DATA
--------------
Board Name:VCU108
Board Revision:1.0
Serial Number:RTK13497603
MAC ID:11:22:33:AA:BB:CC
```

Option 0: Return to Main Menu

This option returns to the menu level above.

CONFIG Menu

The system controller CONFIG menu is used to configure the VCU108 UltraScale FPGA from a micro-SD card. One of sixteen bitstreams can be selected for use by the configuration engine by setting a binary encoded value on the system controller mode DIP switch SW15 positions 1 - 4 (M3, M2, M1, M0) prior to board power up. See FPGA Configuration. Once the board is powered up or when the system controller POR pushbutton (SW14) is pressed, the system controller CONFIG Menu can also be used to select the micro-SD card bitstream.

CONFIG Menu Options

```
VCU108 System Controller
- CONFIG Menu-
1. Configure UltraScale FPGA from microSD Card
0. Return to Main Menu
Select an option
```

Option 1: Configure UltraScale FPGA from microSD Card

```
Enter a Bitstream number (0-15):
0
Info: Xilinx.sys opened
Info Configuration definition file "VCU108d/set0/config.def" opened
Info: Clock divider is set to 2
Info: Total 1 device(s) in the chain
Info: Total 1 configuration target(s) in the chain
Info: Target device ID code: 0x3822093
Info: Target device DNA code: 0xD4B3A5820E041
Info: Configuring target(s)...
Info: Bitfile "VCU108d/set0/ipi_app.bit" opened
...10%...20%...30%...40%...50%...60%...70%...80%...90%...100%
Info: Target Done is high
Info: Target Init_b is high

Configuration completed successfully!
```

Option 0: Return to Main Menu

This option returns to the menu level above.

UltraScale FPGA User Design Considerations

The VCU108 system controller provides simplified access to the programmable features on the VCU108 over an I2C interface. This I2C interface is shared with the UltraScale FPGA and can be driven by an I2C master within a design.

Access to the I2C devices from either the UltraScale FPGA or the system controller takes place over the same shared I2C topology. All I2C accesses go through either the TCA9548 8-port I2C switch or the PCA9544 4-port I2C switch. Designs must deassert the TCA9548 reset (signal IIC_MUX_RESET_B) to access any I2C device attached to one of its eight ports. The PCA9544 4-port I2C switch does not have a reset function.

IMPORTANT: *The TCA9548 U28 RESET_B pin 3 is connected to FPGA U1 bank 64 pin AP10 via level-shifter U44. The PCA9544 U80 does not have a reset pin. FPGA pin AP10 LVCMOS18 net IIC_MUX_RESET_B_LS must be driven High to enable I2C bus transactions with the devices connected to U28.*

Designs that access the SYSMON block over I2C must enable the SYSMON I2C interface and the desired SYSMON channels. See the *UltraScale Architecture System Monitor User Guide (*UG580) [Ref 31] for designing with the SYSMON block.

XILINX

Appendix D

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the VCU108 board provides for designs targeting the VCU108 evaluation board. Net names in the constraints file correlate with net names on the latest VCU108 evaluation board schematic. Users must identify the appropriate pins and replace the net names with net names in the user RTL. See *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 34] for more information.

The FMC connectors J22 (HPC0) and J2 (HPC1) are connected to 1.8V VADJ banks. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT: *The XDC file can be accessed on the* VCU108 Evaluation Kit website.

Board Setup

Installing the VCU108 Board in a PC Chassis

Installation of the VCU108 board inside a computer chassis is required when developing or testing PCI Express® functionality.

When the VCU108 board is used inside a computer chassis (that is, plugged in to the PCIe® slot), power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable shown in Figure E-1 to J15 on the VCU108 board. The Xilinx part number for this cable is 2600304. See [Ref 26] for ordering information.

Figure E-1: **ATX Power Supply Adapter Cable**

To install the VCU108 board in a PC chassis:

1. On the VCU108 board, remove the six screws retaining the six rubber feet with their standoffs, and the PCIe bracket. Reinstall the PCIe bracket using two of the previously removed screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.
5. Plug the VCU108 board into the PCIe connector at this slot.

6. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the VCU108 board in its slot.

Note: The VCU108 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.

7. Connect the ATX power supply to the VCU108 board using the ATX power supply adapter cable as shown in Figure E-1:
   a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J15 on the VCU108 board.
   b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into J15 on the VCU108 evaluation board. The ATX 6-pin connector has a different pinout than J15. Connecting an ATX 6-pin connector into J15 damages the VCU108 evaluation board and voids the board warranty.*

8. Slide the VCU108 board power switch SW1 to the ON position. The PC can now be powered on.

Board Specifications

Dimensions

Height: 6.34 inch (16.10 cm)

Thickness (±5%): 0.061 inch (0.1549 cm)

Length: 10.5 inch (26.7 cm)

IMPORTANT: The VCU108 board height exceeds the standard 4.376 inch (11.15 cm) height of a PCI Express card.

Environmental

Temperature

Operating: 0°C to +45°C
Storage: -25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

Appendix G

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the VCU108 board master answer record concerning the CE requirements for the PC Test Environment:

VCU108 Evaluation Kit – Master Answer Record 62603

CE Directives

2006/95/EC, Low Voltage Directive (LVD)

2004/108/EC, Electromagnetic Compatibility (EMC) Directive

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

IMPORTANT: This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

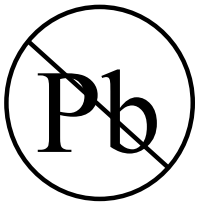
EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.



This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix H

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the VCU108 board and its documentation is available on the following websites.

VCU108 Evaluation Kit

VCU108 Evaluation Kit – Master Answer Record 62603

These Xilinx documents and websites provide supplemental material useful with this guide:

1. *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893)
2. *UltraScale Architecture Configuration User Guide* (UG570)
3. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (Vivado Design Suite)* (PG150)
4. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
5. Micron Technology www.micron.com (EDY4016AABG-DR-F-D, MT44K16M36RB-093E, MT28GU01GAAA1EGC-0SIT)
6. SanDisk: www.sandisk.com
7. SD Association: www.sdcard.org
8. Digilent: www.digilentinc.com (USB JTAG Module, Pmod Peripheral Modules)
9. Silicon Labs: www.silabs.com (Si5335A, Si570, Si53340, Si5328B)
10. *UltraScale Architecture Clocking Resources User Guide* (UG572)
11. SFF-8663 specification: ftp.seagate.com/sff
12. CFP MSA hardware specification: www.cfp-msa.org
13. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
14. *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182)
15. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
16. *UltraScale Devices Gen3 Integrated Block for PCI Express LogiCORE IP Product Guide* (PG156)
17. PCI Express® standard: www.pcisig.com/specifications
18. *Tri-Mode Ethernet MAC LogiCORE IP Product Guide* (PG051)
19. Marvell Semiconductor: www.marvell.com
20. *AXI UART Lite LogiCORE IP Product Guide* (PG142)
21. Analog Devices: www.analog.com/en/index.html (ADV7511KSTZ-P, ADP123, ADG707)

22. *DisplayPort LogiCORE IP Product Guide* (PG064)
23. Texas Instruments: www.ti.com (TCA9548, PCA9544)
24. *Zynq-7000 SoC Overview* (DS190)
25. *Zynq-7000 SoC Technical Reference Manual* (UG585)
26. The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009. Sourcegate only manufactures the latest revision, which is currently A4. To order, contact Aries Ang, aries.ang@sourcegate.net, +65 6483 2878 for price and availability. This is a custom cable and cannot be ordered from the Sourcegate website.
27. Samtec Inc.: www.samtec.com (SEAF series connectors)
28. VITA FMC Marketing Alliance: www.vita.com (FPGA Mezzanine Card (FMC) VITA 57.1 specification)
29. Maxim InTune Digital PowerTool Software Version 1.06.09 is available. Create a Maxim account and login first. www.maximintegrated.com/products/power/intune/
30. *UltraScale Architecture PCB Design User Guide* (UG583)
31. *UltraScale Architecture System Monitor User Guide* (UG580)
32. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
33. *Tera Term Terminal Emulator Installation Guide* (UG1036)
34. *Vivado Design Suite User Guide: Using Constraints* (UG903)
35. *Zynq-7000 SoC PCB Design Guide* (UG933)
36. *Zynq-7000 SoC Packaging and Pinout Product Specification* (UG865)
37. IEEE Standard 802.3-2005 (standards.ieee.org/getieee802)

For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

Please Read: Important Legal Notices

fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos.

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AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.